

1 Features of EasyZapp OTP Programming

This application note describes the available options for programming the AS5040/43/45 including sample C code. Starting with the general permanent programming of the OTP register, it also describes how to do a “soft writing” for single or multiple non-permanent writing of the OTP.

For a detailed description of the AS504x devices, please refer to the dedicated datasheets.

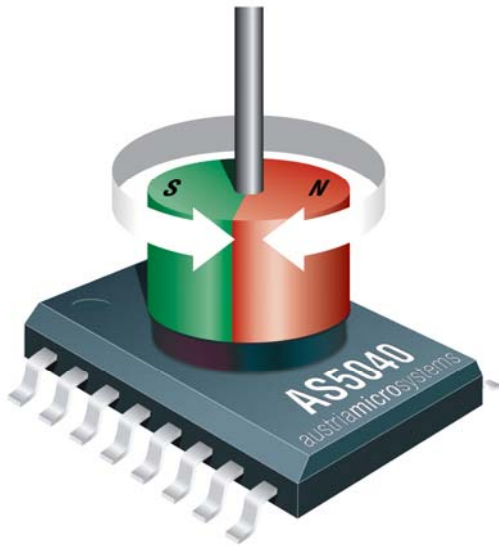


Figure 1: Typical arrangement of AS5040 and magnet

2 OTP Programming

2.1 Hardware Connections

For OTP programming, 3 signals are required: Prog, CSn and CLK. To read the angle position for zero position programming, signal DO is also required. The AS5040 can be programmed in both 3.3V or 5V mode. Figure 2 shows the proper connection in 3.3V mode together with the AS5040 demoboard.

After power-on, programming the AS5040 is enabled with the rising edge of CSn with Prog = high and CLK = low. 16 bit configuration data must be serially shifted into the OTP register via the Prog-pin. The first bit (CCW) is followed by the zero position data (MSB first) and the incremental mode setting as shown in Table 1. Data must be valid at the rising edge of CLK.

After writing data into the OTP register it can be permanently programmed by rising the voltage at pin Prog to the programming voltage VPROG. 16 CLK pulses (IPROG) must be applied to program the fuses (Figure 6). To exit the programming mode, the chip must be reset by a power-on-reset. The programmed data is available after the next power-up.

Note: During the programming process, the transitions in the programming current may cause high voltage spikes generated by the inductance of the connection cable. To avoid these spikes and possible damage to the IC, the connection wires, especially the signals Prog and VSS must be kept as short as possible. The maximum wire length between the VPROG switching transistor and pin Prog (see Figure 2) should not exceed 50mm (2 inches). To suppress eventual voltage spikes, a 10nF ceramic capacitor should be connected close to pins Prog and VSS. This capacitor is only required for programming, it is not required for normal operation.

The clock timing t_{CLK} must be selected at a proper rate to ensure that the signal Prog is stable at the rising edge of CLK. Additionally, the programming supply voltage should be buffered with a 10 μ F capacitor mounted close to the switching transistor. This capacitor aids in providing peak currents during programming. The specified programming voltage at pin Prog is 7.3 – 7.5V. To compensate for the voltage drop across the VPROG switching transistor, the applied programming voltage may be set slightly higher (7.5 – 8.0V, see Figure 2).

*) This application note only applies to encoders with date code later A5xxx!

2.2 EasyZapp OTP Register Contents

The AS5040/43/45 OTP register size is 32 bit and is divided into two sections:

- 16 bits user settings and
- 16 bits factory settings.

The user settings section can be freely modified to fit any application and is described in detail in the following.

The factory settings section of the OTP contains several trimming bits and allows enabling / disabling certain blocks during factory chip testing. The factory settings must not be modified by any means!

2.2.1.1 Assignment of the 16 bit users:

AS5040:

CCW: Counter Clockwise Bit

ccw = 0 – angular value increases in clockwise direction

ccw = 1 – angular value increases in counterclockwise direction

Z [9:0]: Programmable Zero / Index Position

Index: Index Pulse Width: 1LSB / 3LSB

Div1, Div0: Divider Setting of Incremental Out

Md1, Md0: Incremental Output Mode Selection

AS5043:

CCW: Counter Clockwise Bit

ccw = 0 – angular value increases in clockwise direction

ccw = 1 – angular value increases in counterclockwise direction

Z [9:0]: Programmable Zero / Index Position

FB_intEN: OPAMP gain: 0=external, 1=internal

RefExtEN: DAC Ref.: 0=internal, 1=external

ClampMd EN: Analog output span:

0=0-100%*VDD,

1=10-90%*VDD

OR0, OR1: Analog Output Range Selection

[1:0] 00 = 360° 01 = 180°

10 = 90° 11 = 45°

AS5045:

CCW: Counter Clockwise Bit

ccw = 0 – angular value increases in clockwise direction

ccw = 1 – angular value increases in counterclockwise direction

Z [11:0]: Programmable Zero Position

PWM_dis: Disable PWM output

MagCompEn: When set, activates LIN alarm both when magnetic field is too high and too low.

PWMhalfEn: When set, PWM frequency is 122Hz or 2µs / step (when PWMhalfEN = 0, PWM frequency is 244Hz, 1µs/step)

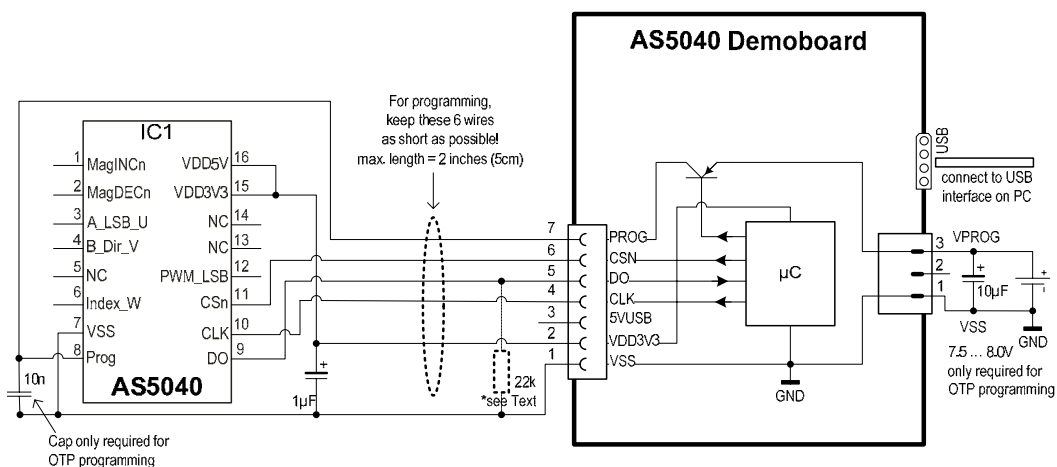


Figure 2: OTP programming connection of AS5040 (shown with AS5040 demoboard)

*) If longer cables are used, a pull-down resistor at the DO line of 22k - 56k Ohms is recommended to discharge the signal between data transmissions and no static voltage is built up.

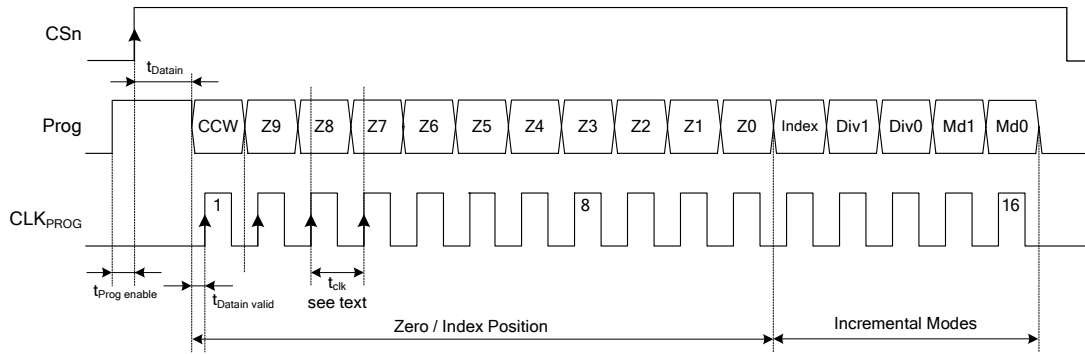


Figure 3: AS5040 Programming access – write data (section of Figure 6)

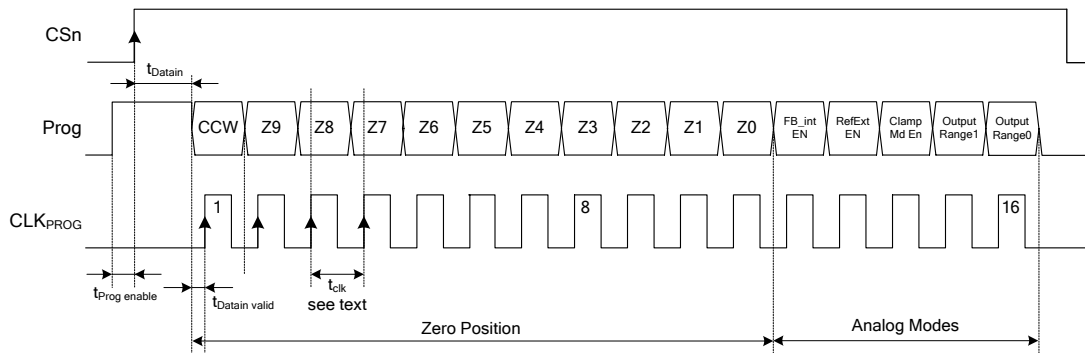


Figure 4: AS5043 Programming access – write data (section of Figure 6)

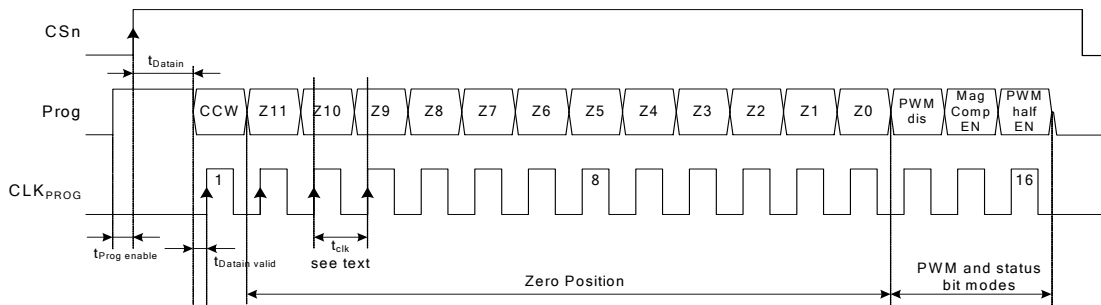


Figure 5: AS5045 Programming access – write data (section of Figure 6)

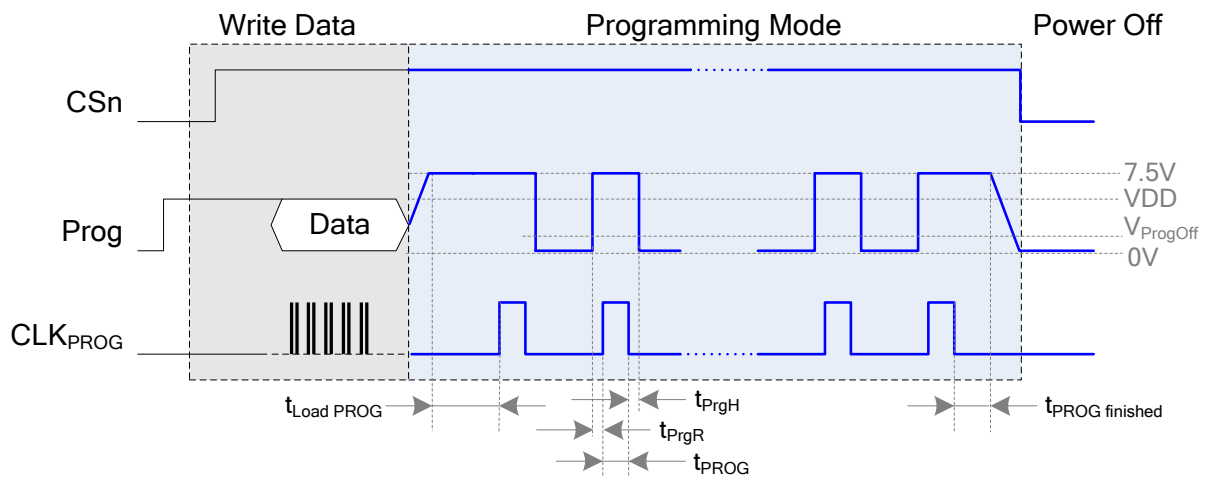


Figure 6: Complete AS504x programming sequence.

2.3 Incremental Mode Programming (AS5040 only)

Three different incremental output modes are available.

Mode: Md1 = 0 / Md0 = 1 sets the AS5040 in quadrature mode.

Mode: Md1 = 1 / Md0 = 0 sets the AS5040 in step / direction mode.

In both modes, the incremental resolution may be reduced from 10 bit down to 9, 8 or 7 bit using the divider OTP bits Div1 and Div0 (see Table 1 below).

Mode: Md1 = 1 / Md0 = 1 sets the AS5040 in brushless DC motor commutation mode with an additional LSB incremental signal at pin 12 (PWM_LSB).

To allow programming of all bits, the default factory setting is all bits = 0. This mode is equal to mode 1:0 (quadrature A/B, 1LSB index width, 256ppr).

The absolute angular output value, by default, increases

with clockwise rotation of the magnet (top view). Setting the CCW-bit allows for reversing the indicated direction, e.g. when the magnet is placed underneath the IC:

CCW = 0 – angular value increases clockwise;

CCW = 1 – angular value increases counterclockwise.

By default, the zero / index position pulse is one LSB wide. It can be increased to a three LSB wide pulse by setting the index-bit of the OTP register.

Further programming options (commutation modes) are available for brushless DC motor-control.

Md1 = Md0 = 1 changes the incremental output pins 3, 4 and 6 to a 3-phase commutation signal. Div1 defines the number of pulses per revolution for either a two-pole (Div1 = 0) or four-pole (Div1 = 1) rotor.

In addition, the LSB is available at pin 12 (the LSB signal replaces the PWM-signal), which allows for high rotational speed measurement of up to 10,000 rpm.

Mode	OTP-Mode-Register-Bit					Pin #				Pulses/Rev ppr	Resolution Bit
	Md1	Md0	Div1	Div0	Index	3	4	6	12		
Default (Mode0.0)	0	0	0*	0*	0*	A	B	1LSB	PWM 10 bit	2x256	10
quadAB-Mode1.0	0	1	0	0	0			1LSB			
quadAB-Mode1.1	0	1	0	0	1			3LSBs			
quadAB-Mode1.2	0	1	0	1	0			1LSB		2x128	9
quadAB-Mode1.3	0	1	0	1	1			3LSBs			
quadAB-Mode1.4	0	1	1	0	0			1LSB			
quadAB-Mode1.5	0	1	1	0	1			3LSBs		2x64	8
quadAB-Mode1.6	0	1	1	1	0			1LSB			
quadAB-Mode1.7	0	1	1	1	1			3LSBs			
Step/Dir-Mode2.0	1	0	0	0	0	LSB	Dir	1LSB	PWM 10 bit	512	10
Step/Dir-Mode2.1	1	0	0	0	1			3LSBs			
Step/Dir -Mode2.2	1	0	0	1	0			1LSB		256	9
Step/Dir -Mode2.3	1	0	0	1	1			3LSBs			
Step/Dir -Mode2.4	1	0	1	0	0			1LSB		128	8
Step/Dir -Mode2.5	1	0	1	0	1			3LSBs			
Step/Dir -Mode2.6	1	0	1	1	0			1LSB		64	7
Step/Dir -Mode2.7	1	0	1	1	1			3LSBs			
Commutation-Mode3.0	1	1	0	0	0	U(0°)	V(120°)	W(240°)	LSB	3 x 1	10
Commutation-Mode3.1	1	1	0	1	0						9
Commutation-Mode3.2	1	1	1	0	0	U' (0°, 180°)	V' (60°, 240°)	W' (120°, 300°)	LSB	2 x 3	10
Commutation-Mode3.3	1	1	1	1	0						9

Table 1: One Time Programmable (OTP) register options

*Note: Div1, Div0 and Index cannot be programmed in Mode 0:0

2.4 Analog Mode Programming (AS5143 only)

The analog output can be configured in many ways:

- It consists of three major building blocks,
- a digital range preselector,
- a 10-bit Digital-to-Analog-Converter (DAC)
- and an OP-AMP buffer stage.

In the default configuration (all OTP bits = 0), the analog output is set for 360° operation, internal DAC reference (VDD5V/2), external OPAMP gain, 0-100% ratiometric to VDD5V.

Shown below is a typical example for a 0°-360° range, 0-5V output. The complete application requires only one external component, a buffer capacitor at VDD3V3 and has only 3 connections VDD, VSS and Vout (connectors 1-3).

Note: the default setting for the OPAMP feedback path is: FB_intEn=0=external. The external resistors Rf and Rg must be installed. In the programmed state (FB_intEn=1=internal), these resistors do not need to be installed as the feedback path is internal (Rf_int and Rg_int).

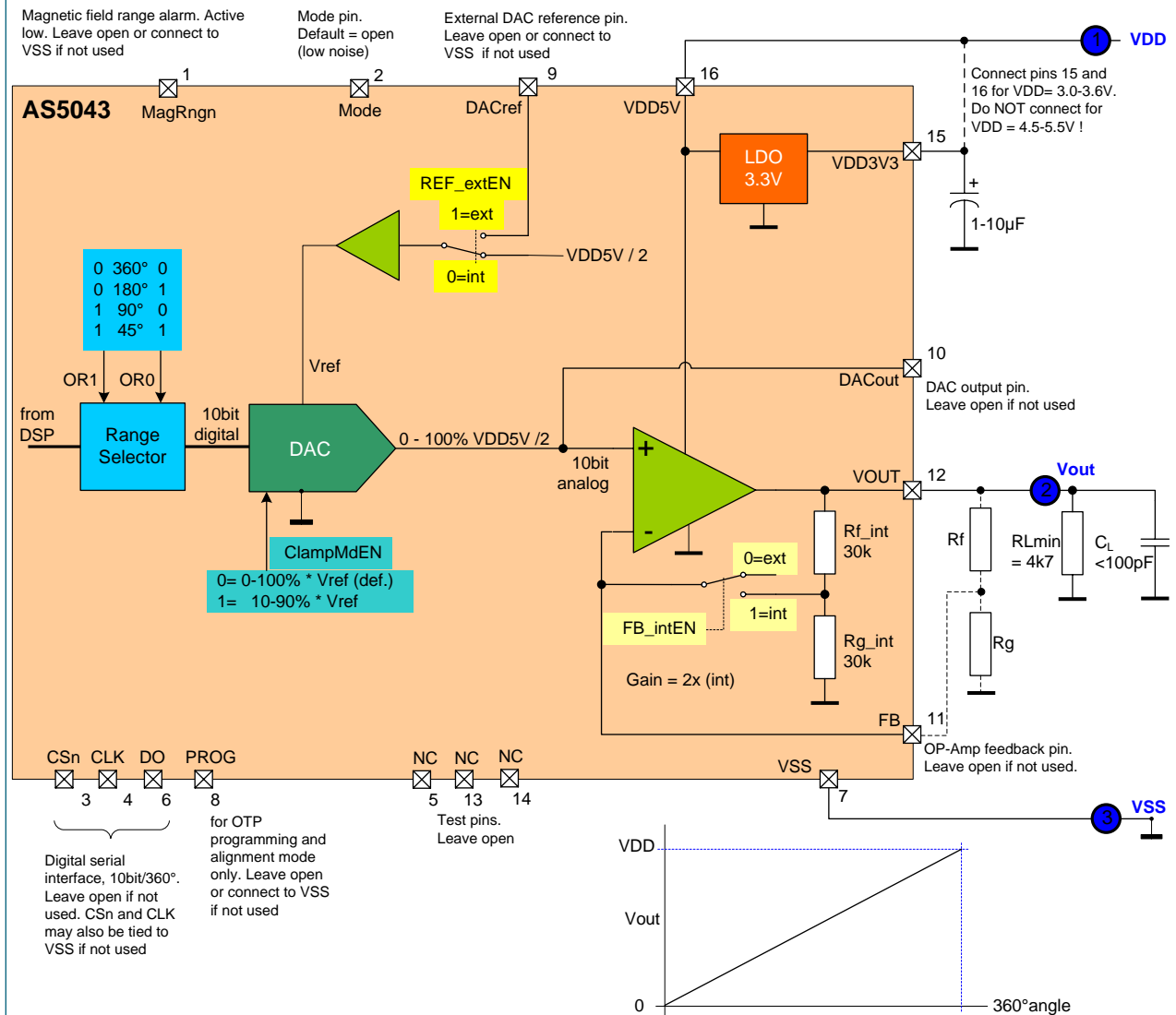


Figure 7: AS5143 analog output block diagram

2.4.1 Angular range Selector (AS5043 only) :

The Angular Range selector allows a digital pre-selection of the angular range. The AS5043 can be configured for a full scale angular range of 45°, 90°, 180° or 360°. In addition, the Output voltage versus angle response can be fine-tuned by setting the gain of the OP-AMP with external resistors and the maximum output voltage can be set in the DAC.

The combination of these options allows configuring the operation range of the AS5043 for all angles up to 360° and output voltages up to 5.5V

The response curve for the analog output is linear for the selected range (45°/90°/180°/360°). In addition, the slope is mirrored at 180° for 45°- and 90°- modes and has a step response at 270° for the 180°-mode. This allows the AS5043 to be used in a variety of applications. In these three modes, the output remains at $V_{out,max}$ and $V_{out,min}$ to avoid a sudden output change when the mechanical angle is rotated beyond the selected analog range. In 360°-mode, a jitter between $V_{out,max}$ and $V_{out,min}$ at the 360° point is also prevented due to a hysteresis.

Output Range1	Output Range0	Mode	Note
0	0	360° angular range (default) 	default mode, analog resolution= 10bit (1024 steps) over 360° analog step size: 1LSB = 0.35°
0	1	180° angular range 	analog resolution= 10bit (1024 steps) over 180° Analog step size: 1LSB = 0.175°
1	0	90° angular range 	analog resolution= 10bit (1024 steps) over 90° Analog step size: 1LSB = 0.088°
1	1	45° angular range 	analog resolution= 9 bit (512 steps) over 45° Analog step size: 1LSB = 0.088°

*) Note: the resolution on the digital SSI interface is always 10bit (0.35°/step) over 360°, independent on analog mode

Table 2: Digital Range Selector programming option

2.4.2 DAC Converter (AS5043 only)

The Digital-to-Analog Converter (DAC) has a resolution of 10bit (1024 steps) and can be configured for the following options:

Internal or external reference

The default DAC reference is the voltage at pin #16 (VDD5V) divided by 2 (see Figure 7). Using this reference, a system that has an output voltage ratiometric to the supply voltage can be built.

Optionally, an external reference source, applied at pin#9 (DACref) can be used. This programming option is useful for applications requiring a precise output voltage that is independent of supply fluctuations, for current sink outputs or for applications with a dynamic reference, e.g. attenuation of audio signals.

0-100% or 10-90% full scale range

The reference voltage for the DAC is buffered internally. The recommended range for the external reference voltage is 0.2V to (VDD3V3 - 0.2)V.

The DAC output voltage will be switched to 0V, when the magnetic field is out of range, when the MagInc and MagDec indicators are both =1 and the MagRngn-pin (#1) will go low.

The default full scale output voltage range is 0-100%*VDD5V. Due to limitations in the output stage of an OP-Amp buffer, it cannot drive the output voltage from 0-100% rail-to-rail. Without load, the minimum output voltage at 0° will be a few millivolts higher than 0V and the maximum output voltage will be slightly lower than VDD5V. With increasing load, the voltage drops will increase accordingly.

As a programming option, an output range of 10-90%*VDD5V can be selected. In this mode, there is no saturation at the upper and lower output voltage limits like in the 0-100% mode and it allows failure detection as the output voltage will be outside the 10-90% limits, when the magnetic field is in the "red" range ($V_{out}=0V$, or when the supply to the chip is interrupted ($V_{out}=0V$ or VDD5V).

The unbuffered output of the DAC is accessible at pin #10 (DACout). This output must not be loaded.

2.4.3 OP-AMP stage (AS5043 only)

The DAC output is buffered by a non-inverting Op-Amp stage. The amplifier is supplied by VDD5V (pin #16) and can hence provide output voltages up to 5V.

By allowing access to the inverting input of the Op-Amp and with the addition of a few discrete components it can be configured in many ways, like high current buffer, current sink output, adjustable angle range, etc...

Per default, the gain of the Op-Amp must be set by two external resistors (see Figure 7). Optionally, the fixed internal gain setting (2x) may be programmed by OTP, eliminating the need for external resistors.

2.4.4 Permanently enabling the analog output (AS5043 only)

An on-chip diagnostic feature turns the analog output off in case of an error (broken supply or magnetic field out of range). This feature can be disabled so the output will not be turned off at week or lost magnetic field.

To enable the analog output permanently the OTP bit FS6 of the factory setting must be set. Figure 12 visualizes the position of the FS6 bit.

2.4.5 Changing the PWM Frequency (AS5045 only)

The PWM frequency of the AS5045 can be divided by two by setting the PWMhalfEN bit of the OTP register. With PWMhalfEN = 0 the PWM timing is as shown in Table 3:

Parameter	Symbol	Typ	Unit	Note
PWM frequency	f_{PWM}	244	Hz	Signal period: 4097 μ s
MIN pulse width	PW_{MIN}	1	μ s	- Position 0d - Angle 0 deg
MAX pulse width	PW_{MAX}	4096	μ s	- Position 4095d - Angle 359,91 deg

Table 3: PWM signal parameters (default mode)

When PWMhalfEN = 1, the PWM timing is as shown in Table 4:

Parameter	Symbol	Typ	Unit	Note
PWM frequency	f_{PWM}	122	Hz	Signal period: 4097 μ s
MIN pulse width	PW_{MIN}	2	μ s	- Position 0d - Angle 0 deg
MAX pulse width	PW_{MAX}	8192	μ s	- Position 4095d - Angle 359,91 deg

Table 4: PWM signal parameters with half frequency (OTP option)

2.4.6 Disabling the PWM output (AS5045 only)

The PWM output can be disabled by setting the PWM_dis bit=1 of the OTP.

2.4.7 Z-axis Range Indication (AS5045 only)

The AS5045 provides several options of detecting movement and distance of the magnet in the Z-direction. Signal indicators MagINCn and MagDECn are available both as hardware pins (pins #1 and 2) and as status bits in the serial data stream (see section 3). Additionally, an OTP programming option is available with bit MagCompEn (see Table 5) that enables additional features.

When bit MagCompEn is programmed in the OTP, the function of status bits MagINC, MagDec and pins MagINCn, MagDECn is changed to the following function:

Status bits			Hardware pins		OTP: Mag CompEn = 1 (red-yellow-green programming option)
Mag INC	Mag DEC	LIN	Mag INCn	Mag DECn	Description
0	0	0	Off	Off	No distance change Magnetic input field OK (GREEN range, -45...75mT)
1	1	0	On	Off	YELLOW range: magnetic field is ~ 25...45mT or ~75...135mT. The AS5045 may still be operated in this range, but with slightly reduced accuracy.
1	1	1	On	On	RED range: magnetic field is ~<25mT or >~135mT. It is still possible to operate the AS5045 in the red range, but not recommended.
All other combinations			n/a	n/a	Not available

Table 5: AS5045 Magnetic field strength red-yellow-green indicator (OTP option)

Note: Pin 1 (MagINCn) and pin 2 (MagDECn) are active low via open drain output and require an external pull-up resistor. If the magnetic field is in range, both outputs are turned off.

The two pins may also be combined with a single pull-up resistor. In this case, the signal is high when the magnetic field is in range. It is low in all other cases (see Table 5).

2.5 Zero Position Programming

Zero position programming is an OTP option that simplifies assembly of a system, as the magnet does not need to be manually adjusted to the mechanical zero position. Once the assembly is completed, the mechanical and electrical zero positions can be matched by software. Any position within a full turn can be defined as the permanent new zero/index position.

For zero position programming, the magnet is turned to the mechanical zero position (e.g. the "off"-position of a rotary switch) and the actual angular value is read.

This value is written into the OTP register bits (Z11) Z9:Z0 and programmed as described in section 2.

This new absolute zero position is also the new index pulse position for incremental output modes.

Note: Programming the CCW bit will cause a shift in the absolute output reading. For this reason, if the CCW and a zero position will be programmed, these operations must be applied separately. As a first step the CCW bit must be set, than the now changed angle can be read and a zero position can be programmed.

The zero position value may also be modified before programming, e.g. to program an electrical zero position that is 180° (half turn) from the mechanical zero position, just add 512 to the value read at the mechanical zero position and program the new value into the OTP register.

2.6 Analog Readback Mode

Non-volatile programming (OTP) uses on-chip zener diodes, which become permanently low resistive when subjected to a specified reverse current.

The quality of the programming process depends on the amount of current that is applied during the programming process (up to 130mA). This current must be provided by an external voltage source. If this voltage source cannot provide adequate power, the zener diodes may not be programmed properly.

In order to verify the quality of the programmed bits, an analog level can be read for each zener diode, giving an indication whether this particular bit was properly programmed or not.

To put the AS5040 in analog readback mode, a digital sequence must be applied to pins CSn, Prog and CLK as shown in Figure 8. The digital level for this pin depends on the supply configuration (3.3V or 5V).

The second rising edge on CSn (OutpEN) changes pin Prog to a digital output and the logic high signal at pin Prog must be removed to avoid collision of outputs (grey area in Figure 8).

The following falling slope of CSn changes pin Prog to an analog output, providing a reference voltage V_{ref} , that must be saved as a reference for the calculation of the subsequent programmed and unprogrammed OTP bits.

Following this step, each rising slope of CLK outputs one bit of data in the reverse order as during programming (see Figure 8: Md0-MD1-Div0,Div1-Idx-Z0...Z9, ccw).

Figure 8 only applies if there is no capacitance at the prog pin. With a capacitance present at the prog pin the speed of analog readout must be reduced depending on the charging behavior of the capacitor.

To enable accelerated analog readback the capacitor at pin Prog (see Figure 2) should be removed.

The measured analog voltage for each bit must be subtracted from the previously measured V_{ref} , and the resulting value gives an indication on the quality of the programmed bit: a reading of <100mV indicates a properly programmed bit and a reading of >1V indicates a properly unprogrammed bit.

A reading between 100mV and 1V indicates a faulty bit, which may result in an undefined digital value, when the OTP is read at power-up. Following the 16th clock (after reading bit "ccw"), the chip must be reset by disconnecting the power supply.

Note: It is not recommended to attempt "cleaning" of a faulty fuse by repeated OTP programming. A chip containing a bad fuse should rather be discarded.

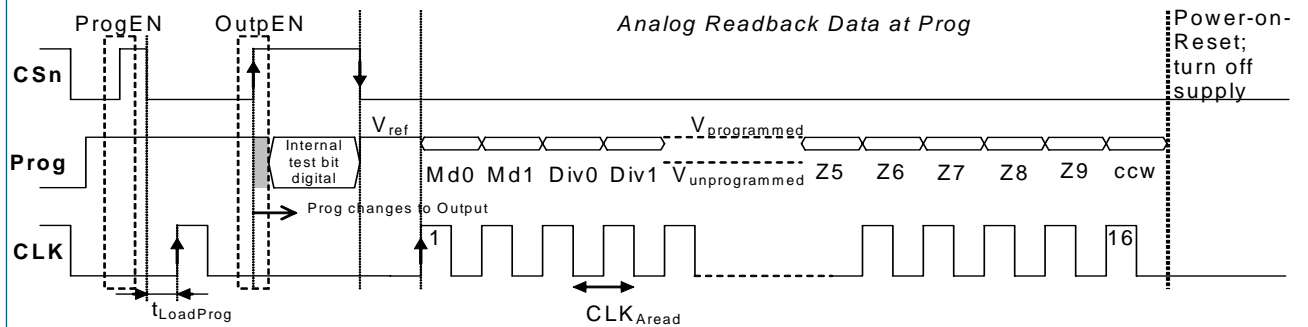


Figure 8: AS5040 16-bit OTP register analog read of user settings

2.6.1 32-bit OTP Analog Read

The 32-bit OTP analog readback sequence is equal to the 16-bit user settings analog readback sequence (see 2.6) except that 32 clocks are applied instead of 16 and an "output disable" sequence is appended instead of a Power-On-Reset.

Note that the order of bits is reversed compared to the digital OTP read sequence (Figure 11). The first bit is MD0, followed by MD1, Div0, Div1, Z0...Z9, CCW, FS15...FS0.

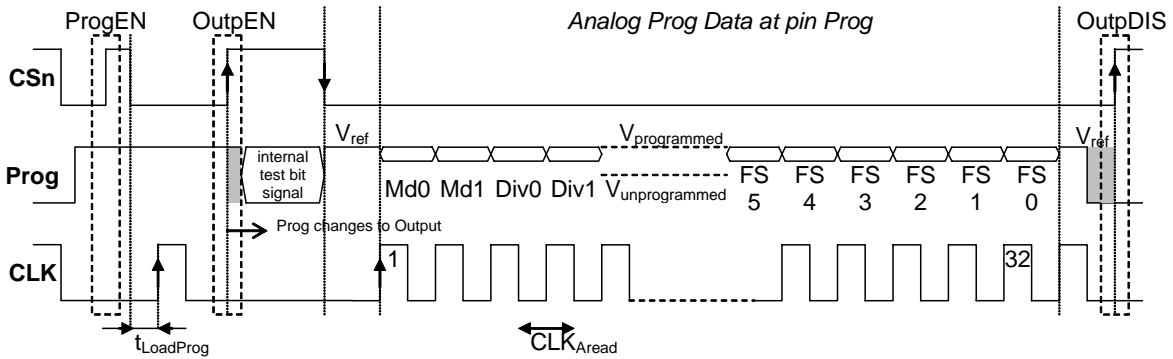


Figure 9: 32-bit OTP analog readback

3 Synchronous Serial Interface (SSI)

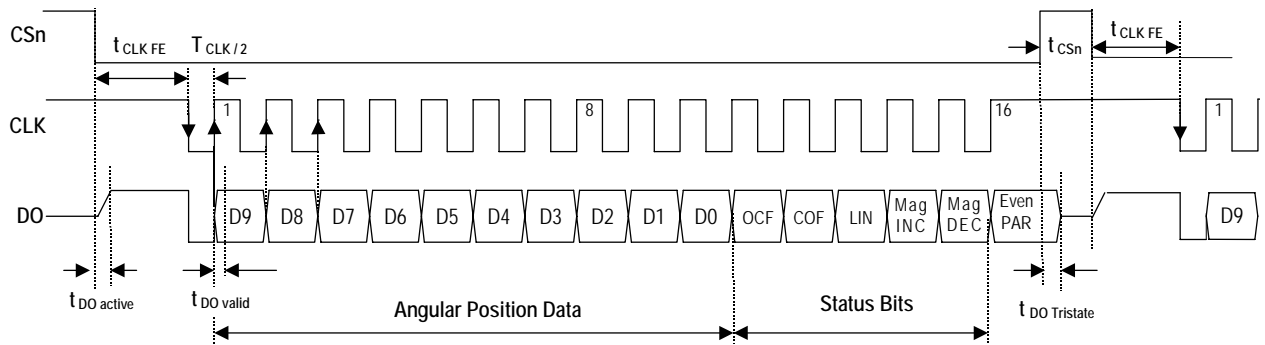


Figure 10: Synchronous serial interface with absolute angular position data

If CSn changes to logic low, Data Out (DO) will change from high impedance (tri-state) to logic high and the read-out will be initiated.

- After a minimum time $t_{CLK FE}$, data is latched into the output shift register with the first falling edge of CLK.
- Each subsequent rising CLK edge shifts out one bit of data.
- The serial word contains 16 bits, the first 10 bits are the angular information D[9:0], the subsequent 6 bits contain system information, about the validity of data such as OCF, COF, LIN, Parity and Magnetic Field status (increase/decrease).
- A subsequent measurement is initiated by a log. "high" pulse at CSn with a minimum duration of t_{CSn} .

For further details on the SSI interface please refer to the dedicated data sheet.

3.1.1 SSI Read Software Implementation

```
void readSSI(BYTE* buffer, BYTE num_bits){
    BYTE current_byte = 0;
    BYTE current_bit = 0;
    BYTE temp = 0;

    CLEAR_CSN();wait(10);//set CSN=0
    CLEAR_CLK(); wait(10);

    temp = 0;
    for(current_bit = num_bits; current_bit; current_bit--){
        SET_CLK();
        temp += (VAL_DO) ? 1 : 0;
        CLEAR_CLK();
        wait(1);
        if(((current_bit - 1) & 0x07) == 0) {
            buffer[current_bit >> 3] = temp;
            temp = 0;
        }
        temp <<= 1;
    }
    SET_CLK();
    SET_CSN();
}
```

4 Non-permanent Writing of the OTP Register

The OTP register may also be written in a non-permanent way (soft write) during operation. This setting is certainly lost with a power-down of the chip. At power-up, the chip is set according to the settings in the OTP register. This setting can be overwritten in two ways:

- Single soft write, if the OTP setting is only overwritten once after power-up of the AS504x
- Repeated soft write, if the OTP setting is overwritten more than once after power-up of the AS5040

4.1 Single OTP Soft Write

If the AS5040/43/45 OTP register is only modified once after power-up, a simplified 16 bit soft write sequence may be applied as shown in Figure 3. This sequence is identical to the first part of the OTP programming sequence, except that CSn, Prog and CLK all return to low after the 16th clock and no programming voltage is applied at pin Prog. This sequence may be followed by a normal angular data read sequence, using CSn, CLK and DO (Figure 10).

Note that this sequence can only be applied once while the AS504x is powered up. To repeat this sequence with a different setting, a power-on-reset must be applied first by cycling the power supply. Repeating this sequence without power-down will overwrite the factory settings and may cause the chip to stop functioning. However, the AS504x will not be permanently damaged by this error state or by improper soft writing. To clear any error state, simply power down / re-start the chip.

4.1.1 OTP Write Software Implementation

```
void writeOTP(BYTE* buffer, BYTE num_bits)
{
    BYTE *current_byte;
    BYTE current_bit = 0;
    BYTE temp = 0;
    current_byte = buffer + ((num_bits-1)>>3);//8 ;
    temp = *current_byte;
    if(num_bits % 8){
        temp <<= 8 - (num_bits % 8);
    }

    OUT_PROG_IN();
    CLEAR_PROG_IN();
    //-- Init OTP-Write
    CLEAR_CSN();
    wait(500);
    CLEAR_CLK();
    wait(500);
    SET_PROG_OUT();
    wait(500);

    SET_CSN();
    wait(500);
    //-- send OTP Data
    for(current_bit = num_bits; current_bit; current_bit--){
        if(temp & 0x80)
            {SET_PROG_OUT();
             wait(600);
            }
        else
            {CLEAR_PROG_OUT();
             wait(600);
            }
        SET_CLK();
        wait(300);// delay
        CLEAR_CLK();
        wait(50);

        temp <<= 1;
        if(((current_bit-1) & 0x07) == 0)
            {
                temp = *--current_byte;
            }
    }
    // END OTP-Write
    CLEAR_PROG_OUT(); // set PROG_OUT=0
    wait(600);

    CLEAR_CSN(); //set CSN=0
    wait(600);
    SET_CSN(); //set CSN=1
    wait(600);
    SET_CLK();
    wait(100);
}
```

4.2 Repeated OTP Soft Write

If the AS5040/43/45 OTP register is to be modified more than once after power-up, the soft write sequence described below must be applied. It requires reading/writing of all 32 bits of the OTP register. It is divided into two sections:

- 16 bits user settings and
- 16 bits factory settings.

4.2.1 OTP User Settings

The user settings section of the OTP contains the bits described in section 2.2: CCW, zero position and incremental mode setting bits. As the name suggests, these bits may be modified and programmed by the user at any possible combination.

4.2.2 OTP Factory Settings

The factory settings section of the OTP contains several trimming bits and allows enabling / disabling certain blocks during factory chip testing. The factory settings must not be modified by any means! An accidental modification of the factory settings in soft write mode can be cleared with a power-on-reset, but a modification of the factory settings during permanent OTP programming may render the chip unusable.

It is therefore recommended to verify the complete OTP register after programming.

Note that each chip may contain a different factory setting!

4.3 Repeated OTP Soft Write Sequence

In order to perform a repeated soft writing of the OTP register, the complete OTP must be read / written and the OTP access sequence must be terminated properly in order to revert to the regular angle reading mode.

The sequence must be as follows:

- Read and store the 32 bit OTP register contents
- Modify the 16 bits of the user settings as required. Make sure not to modify the 16 bits of the factory settings!
- Write the complete 32 bit OTP register with the modified user settings and unmodified factory settings back to the encoder.
- Repeat the OTP write sequence as often as required.

4.3.1 32-bit OTP Register Read Sequence

The complete OTP register read sequence is shown in Figure 11 below. It is initiated with Prog = high and CLK = low at the rising edge of CSn, followed by one dummy clock cycle (CLK #1) with Prog = 1 and CSn = 0 and another rising edge of CSn while Prog = 1. Following this second rising edge of CSn, pin Prog becomes an output and the controller driving pin Prog must change its I/O state from output to input in order to avoid collision of two outputs. The state of Prog is the first bit of the factory settings (FS0). Each subsequent rising edge of CLK shifts out one bit of data. Following the last factory settings bit (FS15) with the 17th clock is the first bit of the user settings (ccw). The 33th clock brings Prog back to 0. The OTP read sequence must be terminated with a pulse on CSn while both Prog and CLK are low.

Note that the OTP read sequence will always read the contents of the "hard programmed" OTP. If you modify the OTP by "soft writing", an OTP read cycle will reset the OTP to the hard programmed values. It can therefore not be used to verify the temporary contents of the OTP after an OTP write cycle (4.3.2).

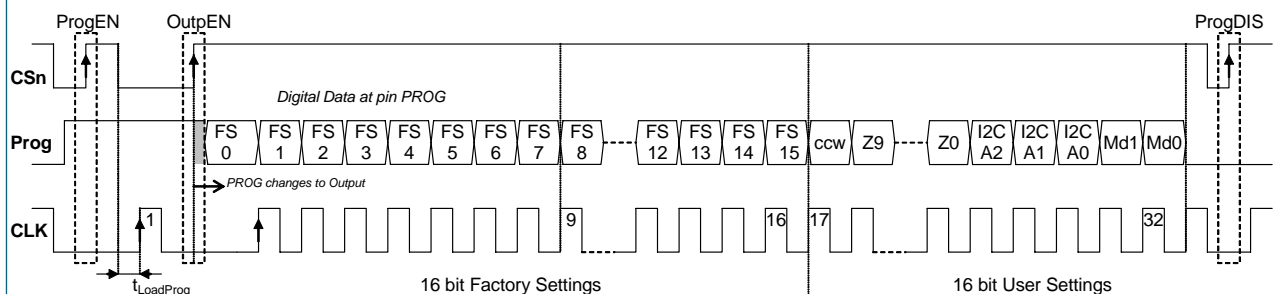


Figure 11: 32-bit OTP register read sequence

4.3.2 32-bit OTP Register Write Sequence

The complete OTP register write sequence is shown in Figure 12 below. Like the OTP read sequence, it is initiated with Prog = high and CLK = low at the rising edge of CSn, but no further pulses are applied at CSn. The programming data must be applied at Prog and is shifted into the OTP with every rising edge of CLK. The sequence of bits is the same as during OTP read: the first bit is factory settings bit 0 (FS0) followed by FS1....FS15.

With the 17th clock, the first bit of the user settings (ccw) is shifted into the OTP register. The sequence is followed by the zero position bits (Z11 or Z9:Z0) and the incremental mode programming bits Indx, Div1, Div0, Md1, Md0. The OTP write sequence must be terminated in the same way as the OTP read sequence: a pulse at CSn while both Prog and CLK are low.

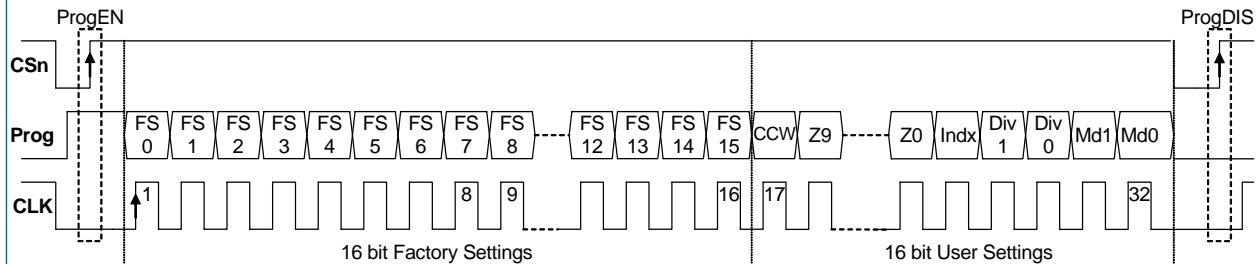


Figure 12: 32-bit OTP register write sequence

This sequence may be repeated as often as required without having to power down the chip between write cycles.

4.4 OTP Register Permanent Write Sequence with Verify

The simplified OTP programming of only the user settings as shown in Figure 6 provides an easy way to program the AS5040/43/45 without having to bother about the contents of the factory settings.

However, in order to make sure that the factory settings have not accidentally been modified during programming of the user settings, it may be a good idea to verify the complete OTP register after programming.

Note: For permanently programming the OTP and for a single soft write, only 16 user bits must be written. The whole 32 bit OTP content including factory settings must be written for repeated temporary writing the OTP only.

The read-write-verify sequence would be as following:

- Write the 16 user bits containing the wanted settings to the OTP register like shown in Figure 12.
- Initiate a programming cycle with a rising slope at CSn and VPROG = 7.3 – 7.5 Volts (middle section of Figure 6). Apply 16 pulses at CLK of 2µs +/- 10% length while VPROG is applied. This procedure will program each OTP bit that contains a "1". OTP bits containing a "0" will not be programmed.
- After programming is completed, set Prog to 0 and verify the programmed data as shown in Figure 11. Alternatively, you may use the 32-bit OTP analog readback sequence (Figure 8) that allows you to also verify the quality of the programmed and unprogrammed fuses. The complete write-program-verify sequence is shown in Figure 13.

4.4.1 OTP Program Software Implementation.

```

void zappOTP(BYTE* buffer, BYTE num_bits)
{
    BYTE counter = 0;
    CLEAR_CSN(); //set CSN=0
    wait(10);
    CLEAR_CLK();
    wait(10);

    // Init Zapping Mode
    SET_V_ZAPP(); // set V_ZAPP = 1
    wait(100);

    SET_CSN(); //set CSN=1
    wait(50);

    // start zapping
    //num_bits = 32;
    for(counter = 0; counter <= num_bits; counter++){
        SET_CLK(); //set CLK=1
        _nop_(); // wait for tzapp = 2us (typ.) High periode
        CLEAR_CLK(); //set CLK=0
        wait(1);

        CLEAR_V_ZAPP(); // set V_ZAPP = 1
        OUT_PROG_IN();
        CLEAR_PROG_IN();
        wait(80);
        INP_PROG_IN();
        _nop_();
        SET_V_ZAPP(); // set V_ZAPP = 1
        wait(1);
    }

    // End Zapping Mode
    CLEAR_V_ZAPP(); // set V_ZAPP = 0

    OUT_PROG_IN();
    CLEAR_PROG_IN();

    wait(200);

    INP_PROG_IN();
    _nop_();

    CLEAR_CSN(); //set CSN=1
    wait(2);
    SET_CSN(); //set CSN=1
    wait(2);
    CLEAR_CSN(); //set CSN=1
}
    
```

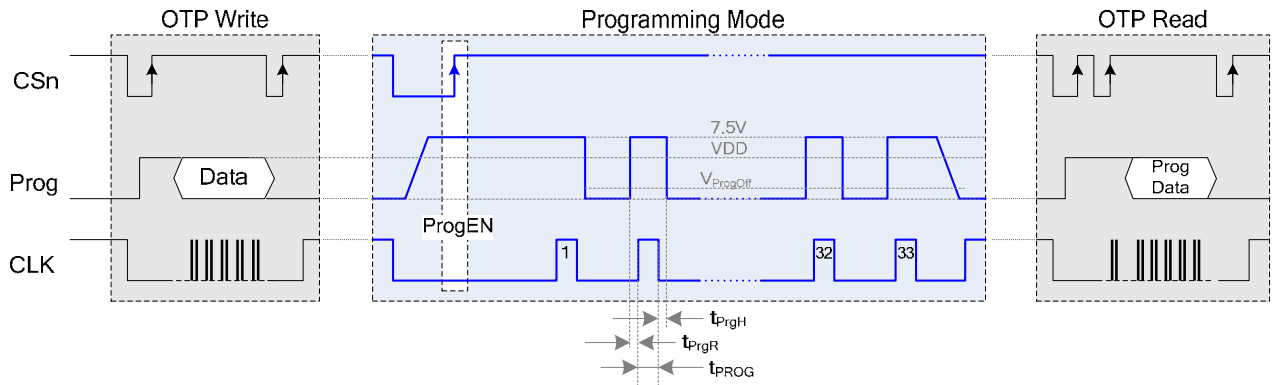


Figure 13: Permanent programming and verification of complete OTP register

5 Repeated Permanent Programming

You may apply the OTP “hard programming” sequence (Figure 6, Figure 13) more than once, but you can only change a “0” to a “1”, it is not possible to hard program a “1” back to “0”. If you must repeat the permanent (“hard”) programming sequence on an already programmed chip, you should only set those bits to “1” that need to be modified from “0” to “1”.

Bits that already contain a “1” in the OTP should not be set to “1” during programming again, as this would apply a programming current to an already programmed fuse.

6 Programming Conditions

Table 6 shows the required parameters for programming the AS5040/43/45. Please refer to the dedicated datasheets for the complete list of operating parameters.

(operating conditions: $T_{amb} = -40$ to $+125^{\circ}\text{C}$, $V_{DD5V} = 3.0$ - 3.6V (3V operation) $V_{DD5V} = 4.5$ - 5.5V (5V operation) unless otherwise noted)

Parameter	Symbol	Min	Typ	Max	Unit	Note
Programming enable time	$t_{\text{Prog enable}}$	2			μs	Time between rising edge at Prog pin and rising edge of CSn
Write data start	$t_{\text{Data in}}$	2			μs	
Write data valid	$t_{\text{Data in valid}}$	250			ns	Write data at the rising edge of CLK_{PROG}
Load programming data	$t_{\text{Load PROG}}$	3			μs	
Rise time of V_{PROG} before CLK_{PROG}	t_{PrgR}	0			μs	
Hold time of V_{PROG} after CLK_{PROG}	t_{PrgH}	0		5	μs	
Write data – programming CLK_{PROG}	CLK_{PROG}			250	kHz	
CLK pulse width	t_{PROG}	1.8	2	2.2	μs	During programming; 16 clock cycles
Hold time of V_{prog} after programming	$t_{\text{PROG finished}}$	2			μs	Programmed data is available after next power-on
Programming voltage	V_{PROG}	7.3	7.4	7.5	V	Must be switched off after zapping
Programming voltage off level	V_{ProgOff}	0		1	V	Line must be discharged to this level
Programming current	I_{PROG}			130	mA	During programming
Analog read CLK	$\text{CLK}_{\text{Aread}}$			100	kHz	Analog readback mode
Programmed zener voltage (log.1)	$V_{\text{programmed}}$			100	mV	$V_{\text{Ref}} - V_{\text{PROG}}$ during analog readback mode (see 2.6)
Unprogrammed zener voltage (log. 0)	$V_{\text{unprogrammed}}$	1			v	

Table 6: Programming parameters

7 Revision History

Revision	Date	Description
1.0	Aug. 23, 2006	Initial revision

8 Contact

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