

1 AS5043 Application examples

The AS5043 is a contactless magnetic angle encoder for accurate measurement up to 360°.

It provides a digital 10-bit as well as a programmable analog output that is directly proportional to the angle of a magnet, rotating over the chip.

The analog output can be configured in many ways, including user programmable angular range, adjustable output voltage range, voltage or current output, etc..

The following pages describe several application examples for the analog output. For a detailed description of the AS5043, please refer to the AS5043 datasheet.

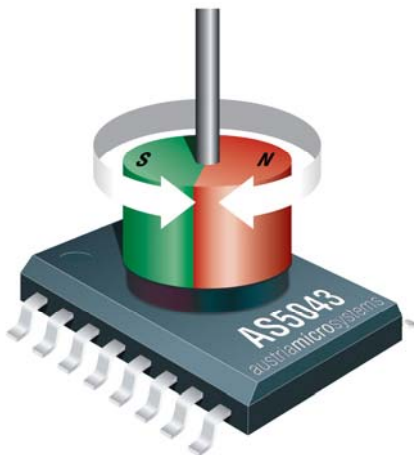


Figure 1: Typical arrangement of AS5043 and magnet

1.1 Pin Configuration

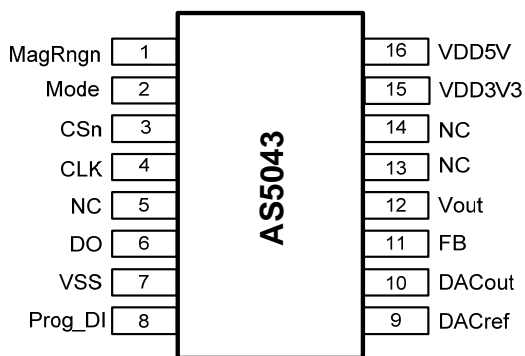


Figure 2: AS5043 pin configuration SSOP16

Pin	Symbol	Type	Description
1	MagRngn	DO_OD	Magnet Field Magnitude RaNGe warning; active low, indicates that the magnetic field strength is outside of the recommended limits.
2	Mode	DI_PD, ST	Mode input. Select between low noise (open, low) and high speed (high) mode. Internal pull-down resistor
3	CSn	DI_PU, ST	Chip Select, active low; Schmitt-Trigger input, internal pull-up resistor (~50kΩ)
4	CLK	DI,ST	Clock Input of Synchronous Serial Interface; Schmitt-Trigger input
5	NC	-	must be left unconnected
6	DO	DO_T	Data Output of Synchronous Serial Interface
7	VSS	S	Negative Supply Voltage (GND)
8	Prog_DI	DI_PD	OTP Programming Input and Data Input for Daisy Chain mode. Internal pull-down resistor (~74kΩ). Should be connected to VSS if not used
9	DACref	AI	DAC Reference voltage input for external reference
10	DACout	AO	DAC output (unbuffered, Ri ~8kΩ)
11	FB	AI	Feedback, OPAMP inverting input
12	Vout	AO	OPAMP output
13	NC	-	Must be left unconnected
14	NC	-	Must be left unconnected
15	VDD3V3	S	3V-Regulator Output for internal core, regulated from VDD5V. Connect to VDD5V for 3V supply voltage. Do not load externally.
16	VDD5V	S	Positive Supply Voltage, 3.0 to 5.5 V

Table 1: Pin description SSOP16

DO_OD	digital output open drain	S	supply pin
DI_PD	digital input pull-down	DO_T	digital output /tri-state
DI_PU	digital input pull-up	ST	schmitt-trigger input
AI	analog input	AO	analog output
DI	digital input		

1.2 AS5043 block diagram

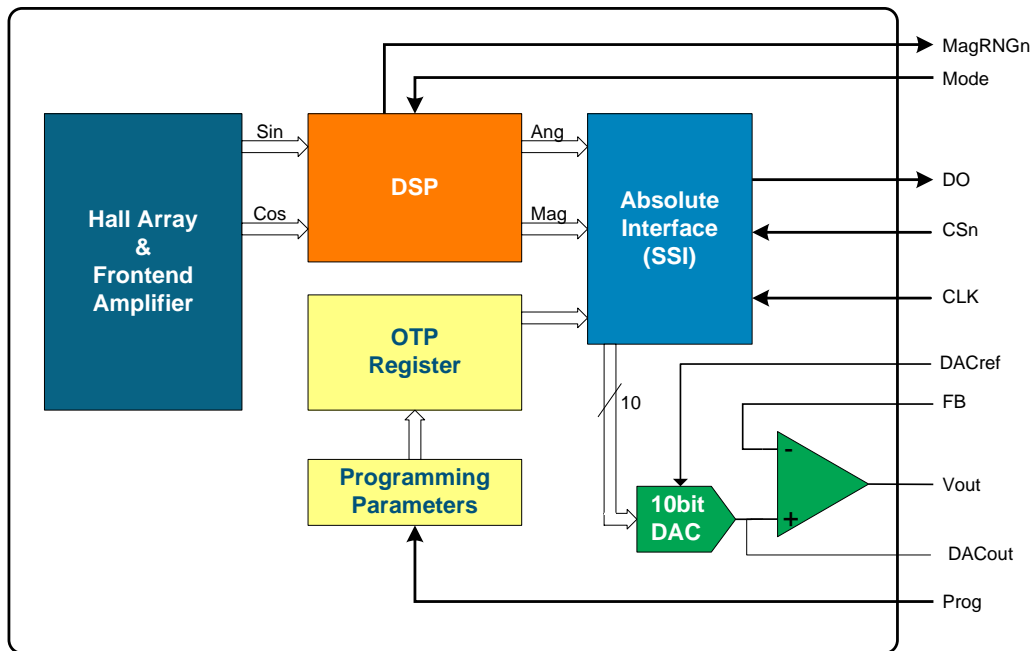


Figure 3: AS5043 block diagram

2 3.3V / 5V Operation

The AS5043 operates either at 3.3V $\pm 10\%$ or at 5V $\pm 10\%$. This is made possible by an internal 3.3V Low-Dropout (LDO) Voltage regulator. The core supply voltage is always taken from the LDO output, as the internal blocks are always operating at 3.3V.

For 3.3V operation, the LDO must be bypassed by connecting VDD3V3 with VDD5V (see Figure 4).

For 5V operation, the 5V supply is connected to pin VDD5V, while VDD3V3 (LDO output) must be buffered by a 1...10 μ F capacitor, which should be placed close to the supply pin (see).

The VDD3V3 output is intended for internal use only. It should not be loaded with an external load.

The voltage levels of the digital interface I/O's correspond to the voltage at pin VDD5V, as the I/O buffers are supplied from this pin (see Figure 4).

A buffer capacitor of 100nF is recommended in both cases close to pin VDD5V.

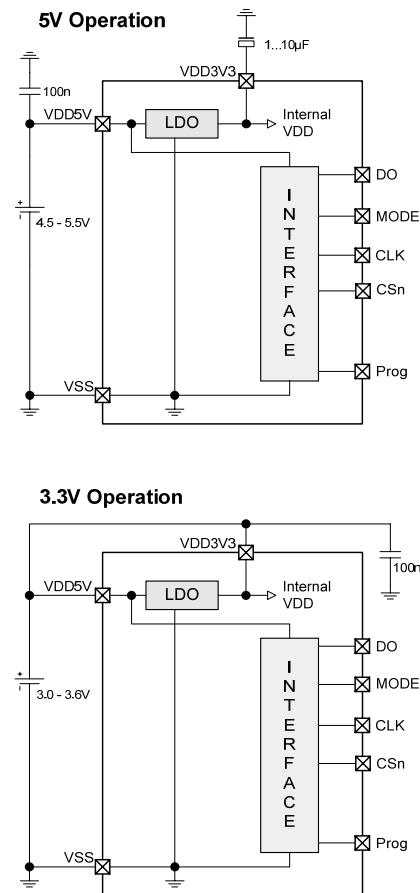


Figure 4: Connections for 5V / 3.3V supply voltages

3 AS5043 programming

After power-on, programming the AS5043 is enabled with the rising edge of CSn and Prog = logic high. 16 bit configuration data must be serially shifted into the OTP register via the Prog-pin. The first "CCW" bit is followed by the zero position data (MSB first) and the Analog Output Mode setting (see Datasheet). Data must be valid at the rising edge of CLK (see Figure 5). Following this sequence, the voltage at pin Prog must be raised to the programming voltage V_{PROG} (see Figure 6). 16 CLK pulses (t_{PROG}) must be applied to program the fuses. To exit the programming mode, the chip must be reset by a power-on-reset. The programmed data is available after the next power-up.

OTP Register Contents:

CCW Counter Clockwise Bit
 ccw=0 – angular value increases with clockwise rotation
 ccw=1 – angular value increases with counterclockwise rotation

Z [9:0] Programmable Zero / Index Position

FB_intEN OPAMP gain setting: 0=external, 1=internal

RefExtEN DAC reference: 0=internal, 1=external

ClampMd EN Analog output span: 0=0-100%, 1=5-95%*VDD

Output Range Analog Output Range Selection

[1:0]	00 = 360°	01 = 180°
	10 = 90°	11 = 45°

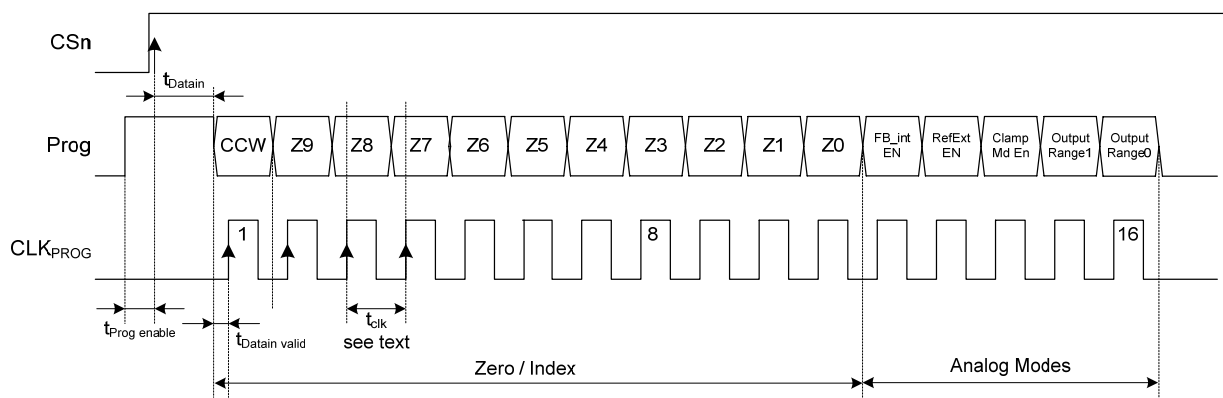


Figure 5: Programming Access – OTP Write Cycle (section of Figure 6)

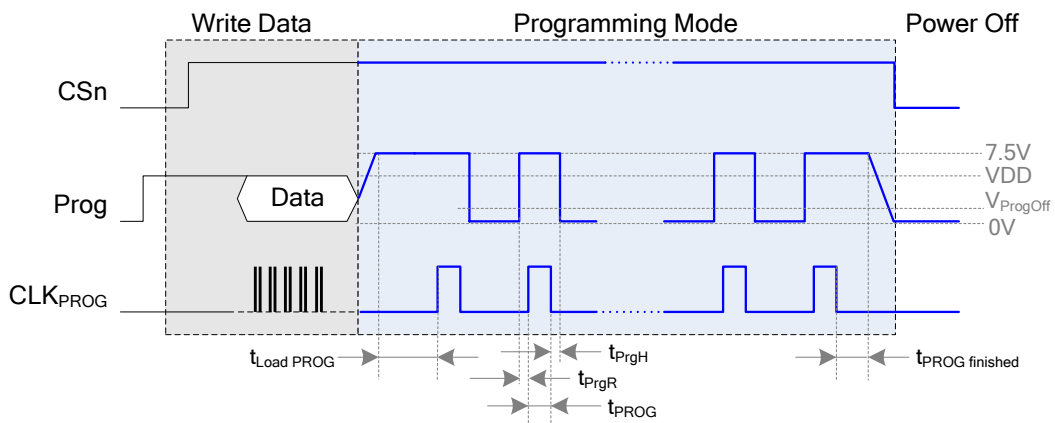


Figure 6: Complete OTP programming sequence

Further information on programming can be found in the AS5043 Datasheet and in Application Note AN5000-20. Both documents are available for download at the austriamicrosystems. website: www.austriamicrosystems.com

4 Application Examples

4.1 Application Example 1: Default configuration

The chip is shipped with the default, unprogrammed configuration, when all OTP bits are zero. The corresponding analog configuration is:

REF_extEN = 0 : DAC reference (Vref) is VDD5V/2
 OR1, OR0 = 00 : selected angular range = 10 bit over 360°, resolution = 0.35° per step
 ClampMdEN = 0 : DAC output voltage is (0 – 100%)*Vref = (0 – 50%)*VDD5V
 „FB_intEN“ = 0 : OPAMP gain is external, using Rf and Rg

The resulting output voltage is ratiometric to VDD:
 $V_{out} = 2x (0...50\%)VDD5V = V_{out} = (0...100\%)VDD5V$.

Figure 7 below shows all pins and their default connection. For clarity, unused pins will not be shown in the subsequent application examples. A detailed pin description can be found in Table 1 and in the AS5043 datasheet.

For this configuration, only a buffer capacitor at pin VDD3V is required, the complete circuit requires only 3 wires: VDD, VSS and Vout (Connectors 1-3 on the right hand side of Figure 7).

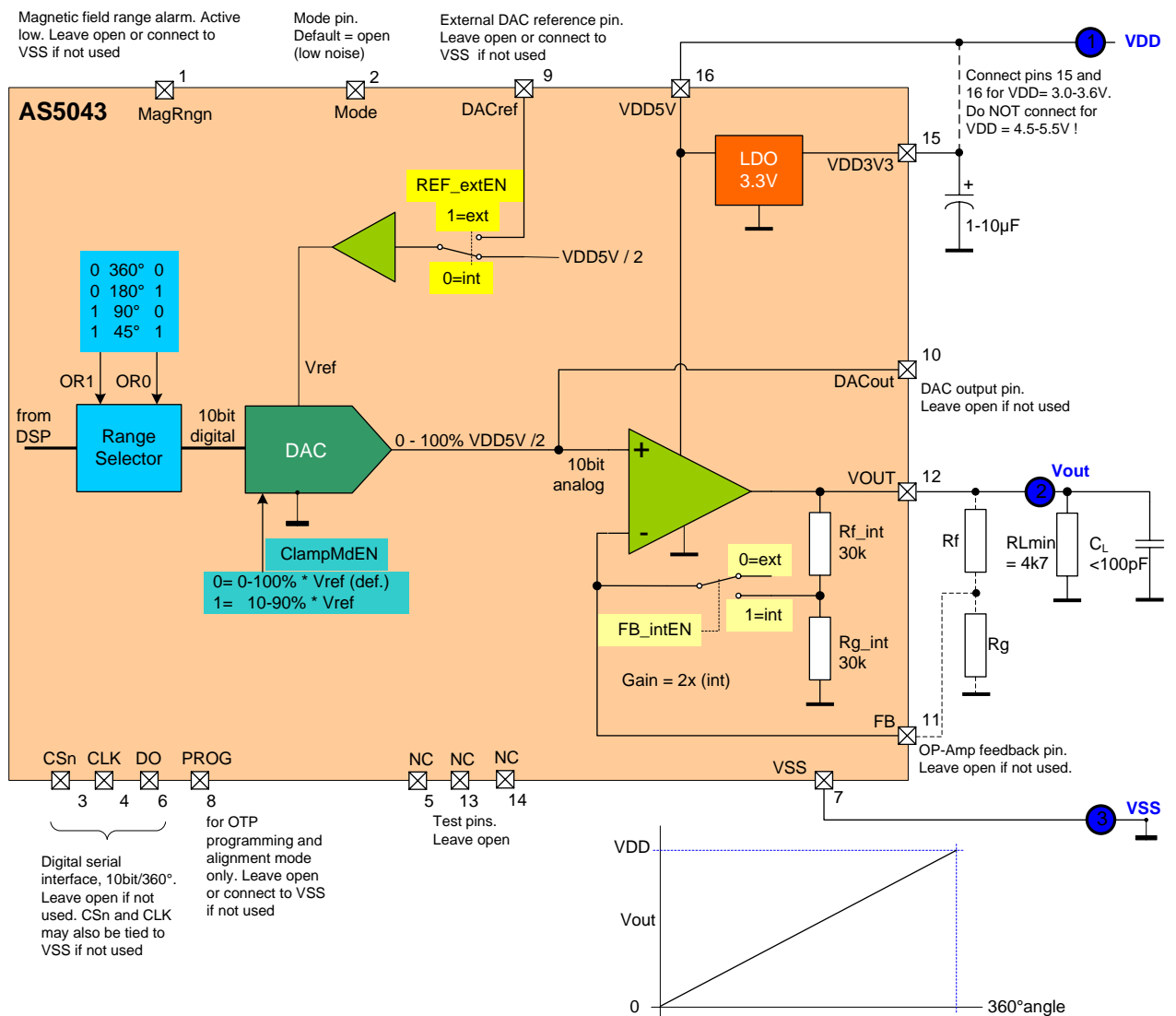


Figure 7: AS5043 default configuration

4.2 Application Example 2: 180° angular range with voltage clamping

This is a typical example of an application requiring less than 360° angular operating range, e.g. a valve position sensor. In order to detect a broken supply, the output voltage in normal operation is clamped to (5...95%)VDD. In case of a broken supply, the output voltage would be below 5%VDD or above 95%VDD, depending on whether pull-up or pull-down resistors are installed at the receiving side. The AS5043 is configured for 5V supply, VDD5V is 5V.

See Figure 7 for unused pin connections.

REF_extEN = 0 : DAC reference (Vref) is VDD5V/2
 OR1, OR0 = 01 : selected angular range = 10 bit over 180°, resolution = 0.176° per step
 ClampMdEN = 1 : DAC output voltage is (10 – 90%)*Vref = (5 – 45%)*VDD5V
 „FB_intEN“ = 1 : OPAMP gain is internal, fixed to 2x

The resulting output voltage is ratiometric to VDD:

$$V_{out} = 2x (5...45\%)VDD5V = V_{out} = (10...90\%)VDD5V = 0.5 \dots 4.5V$$

For this configuration, only a buffer capacitor at pin VDD3V is required, the complete circuit requires only 3 wires:

VDD, VSS and Vout.

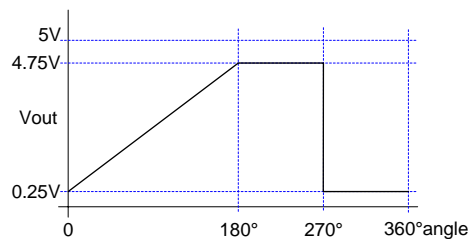
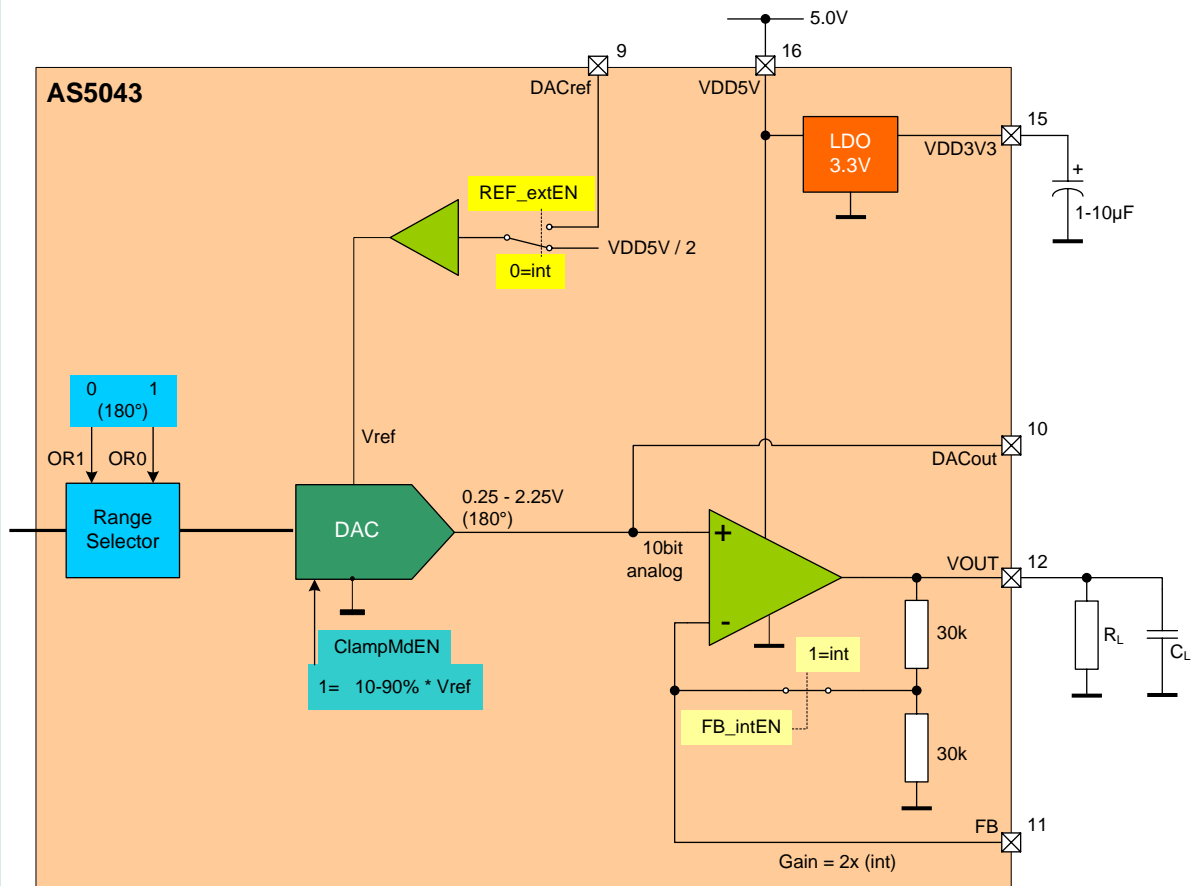


Figure 8: 180° operating angle with clamping

4.3 Application Example 3: angular sub-range adjustment

This is an example for a sub-range application, which is outside of the fixed ranges (45°/90°/180°/360°). As an example, an angular range of 75° with an output voltage range of 0V...5V, ratiometric to VDD is assumed. The following rules can be applied to any sub-range setting:

- Step1: select the power supply configuration (3.3V / 5V):**
since the required maximum output voltage is >3.3V, use the 5V supply configuration: (see Figure 4)
- Step2: set the maximum output voltage:**
since the required maximum output voltage should be ratiometric to VDD, the internal DAC reference VDD5V/2 is selected. By OTP option, the maximum output voltage can be set by an external reference at pin DACref
- Step3: select the angular range (45°/90°/180°/360°):**
since this application example is none of the fixed ranges, select the next higher range: for 75° select 90°
- Step4: set the desired angular range by adjusting the OPAMP gain:**
In 90° mode, the analog output is configured for 1024 steps over 90°, which corresponds to 853 steps over 75°. The internal DAC reference (= maximum DAC output voltage) is VDD5V / 2 = 2.5V @ 90°. The desired maximum output voltage is 5V @ 75°

This corresponds to an OPAMP gain of $gain = \frac{V_{OUT,max} * max_step_size}{V_{IN,max} * subrange_step_size} = \frac{5V * 1024}{2.5V * 853} = 2.4$

To adjust this gain, calculate the gain setting resistors R_F and R_G. R_F should not be too small to avoid unnecessary loading of the OPAMP output. A typical value for R_F is ~10...50kΩ. Since the OPAMP output stage is configured as a noninverting amplifier, the OPAMP gain is calculated as:

$$gain = 1 + \frac{R_F}{R_G}$$

Assuming a value of 33kΩ for R_F, R_G would be: $R_G = \frac{R_F}{gain-1} = \frac{33k\Omega}{2.4-1} = 23,6k\Omega$

Result: The OPAMP is configured as a basic non-inverting amplifier.

The AS5043 is configured for 5V supply, VDD5V is 5V and VDD3V3 is buffered.. See Figure 7 for unused pin connections.

- REF_extEN = 0 : DAC reference (Vref) is VDD5V/2
- OR1, OR0 = 10 : selected angular range = 10 bit over 90°, resolution = 0.088° per step , 853 steps for 75°
- ClampMdEN = 0 : DAC output voltage is (0 – 100%)*Vref = (0 – 50%)*VDD5V
- „FB_intEN“ = 0 : OPAMP gain is external, R_F=33kΩ, R_G=23,6kΩ (22kΩ+1,6kΩ in series)

For this configuration, 2 decoupling capacitors (VDD3V3, VDD5V) and 2-3 resistors for the gain setting (R_F,R_G) are required, the complete circuit requires only 3 wires:VDD, VSS and Vout.

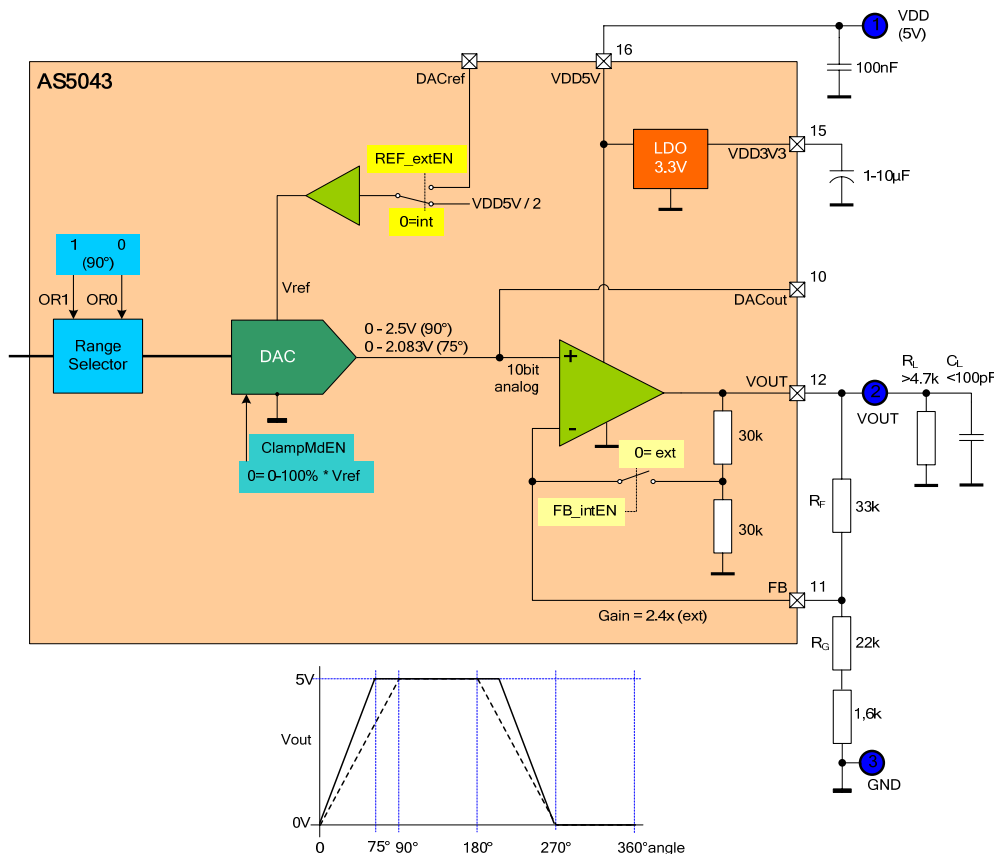


Figure 9: adjustment of angular sub-range

4.4 Application Example 4: angular range and deadzone adjustment

This is a typical example for a potentiometer replacement with an angular range of 275°. Since this angular range is not one of the fixed ranges (45°, 90°, 180° or 360°), the angular range selector is set to the next higher range (360°) and the slope of the output voltage versus angle response is obtained by adjusting the gain of the OPAMP externally. In addition, an angular offset is added to avoid jumping from $V_{out,min}$ to $V_{out,max}$ when the sensor magnet is rotated counterclockwise beyond the mechanical zero position.

The OPAMP is configured as a non-inverting amplifier with a bias (=offset) voltage.

The AS5043 is configured for 3.3V supply, VDD5V is 3.3V. See Figure 7 for unused pin connections.

- REF_extEN = 0 : DAC reference (Vref) is VDD5V/2
- OR1, OR0 = 00 : selected angular range = 10 bit over 360°, resolution = 0.35° per step , 782 steps for 275°
- ClampMdEN = 0 : DAC output voltage is (0 – 100%)*Vref = (0 – 50%)*VDD5V
- „FB_intEN“ = 0 : OPAMP gain is external

Vout can be calculated as:
$$V_{OUT} = V_{IN} * \left[1 + R_F \left(\frac{R_B + R_G}{R_B * R_G} \right) \right] - \frac{V_B R_F}{R_B}$$
 where V_{IN} is the DAC output voltage

The resulting output voltage is ratiometric to VDD in the range of 30° to 305° (span = 275°). The matching of the mechanical zero position to the beginning of the slope is done by software simply by moving the electrical zero position to the mechanical -30° point (move to mechanical zero position, read value, subtract (1024*30/360=85), write result in OTP). After OTP programming, the final sensor will provide a ratiometric output voltage from 0V-VDD5V in the range of 0- 275 mechanical degrees. It will stay at 0V from -30° to 0° and at VDD5V from 275° - 330°.

For this configuration, a buffer capacitor at pin VDD3V, two resistors for the gain setting (R_F, R_G) and one resistor for the angular offset (R_B) are required, the complete circuit requires only 3 wires:VDD, VSS and Vout.

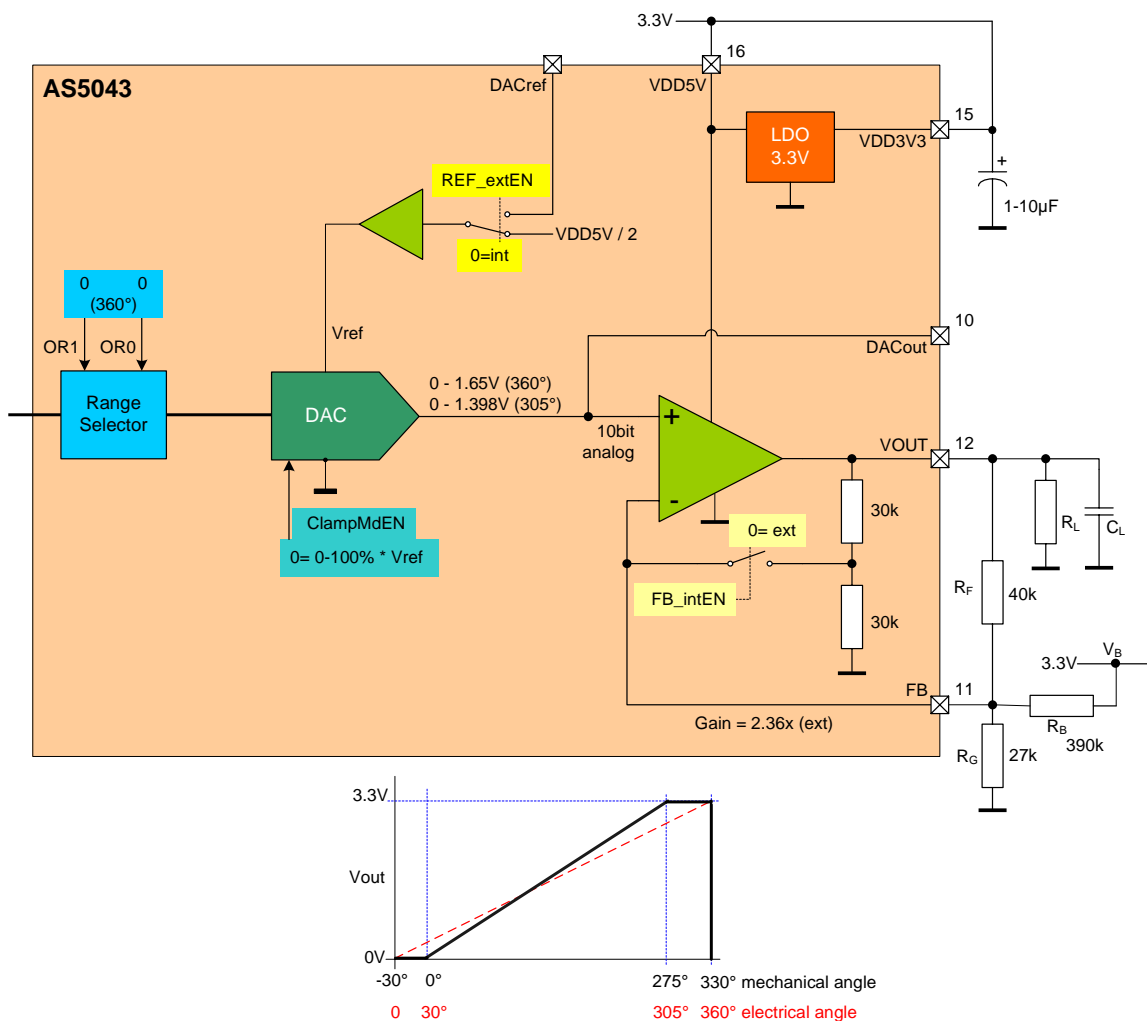


Figure 10: adjustment of angular range + deadzone

4.5 Application Example 5: buffered output

The AS5043 can drive loads of typically 1mA in normal operation without degrading performance. If more load current is required, a simple buffer transistor as shown in Figure 11 below is recommended. Since the OPAMP output voltage V_{out} must be $1V_{BE}$ (~0.7V) higher than the required load voltage, this circuit cannot drive load voltages up to the rails. In this example, the AS5035 is supplied with 5 Volts and the output voltage is specified for $(10...90\%)*3.3V = 0.33V \dots 2.97V$. For this configuration, a gain of $(3.3V/2.5V) = 1.32x$ is required, set by two external resistors (2.4k and 7.5k). The angular range in this example is 90° . See Figure 7 for unused pin connections.

- REF_extEN = 0 : DAC reference (Vref) is VDD5V/2
- OR1, OR0 = 10 : selected angular range = 10 bit over 90° , resolution = 0.088° per step ,
- ClampMdEN = 1 : DAC output voltage is $(10 - 90\%)*V_{ref} = (5 - 45\%)*V_{DD5V}$
- „FB_intEN“ = 0 : OPAMP gain is external, 1.32x.

The resulting output voltage is ratiometric to VDD: $V_{out} = (10...90\%)*(V_{DD5V} / 2)*1.32 = 0.33...2.97V$ from 0° to 90°

For this configuration, a buffer capacitor at pin VDD3V3 and two resistors for the gain setting and a general purpose bipolar NPN transistor are required, the complete circuit requires only 3 wires:VDD, VSS and V_{out} . It can drive loads of 100mA or more, depending on the gain of the buffer transistor.

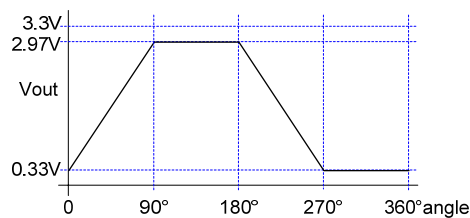
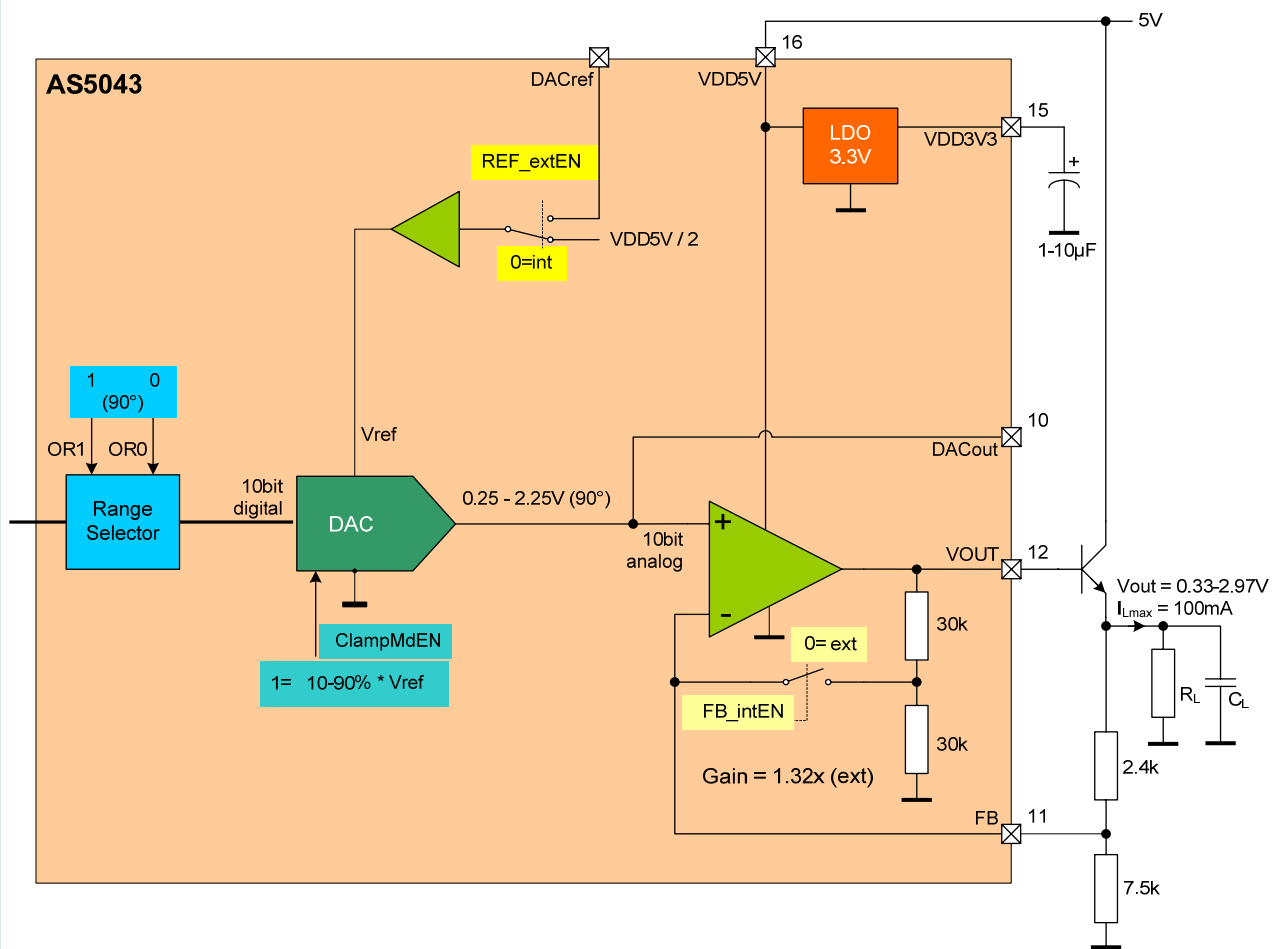


Figure 11: output voltage buffer

4.6 Application Example 6: current output

The AS5043 output can also be configured for an angular proportional current output. The advantage of a current output is that it is over a wide range independent of the load resistance. Consequently, the output current will not be affected by contact resistances of connectors or long wires.

The current source is built by a bipolar transistor at Vout with a fixed emitter resistor. The emitter voltage is fed back to the inverting input of the OPAMP. The resulting output current is V_{DAC} / R_E . V_{DAC} is proportional to the angle; the maximum DAC output voltage in this case is 1.2V, taken from pin DACref. The external DAC reference voltage has the advantage that the resulting current is independent of fluctuations on the supply voltage.

The load is connected between the collector of the bipolar transistor and an external positive supply voltage. This voltage can be up to 50V or even more, depending on the breakdown voltage of the transistor.

The angular range in this example is 360°, the maximum load current is $(1.2V / 60\Omega) = 20mA$.

- REF_extEN = 1 : DAC reference (Vref) is external 1.2V, taken from pin DACref
- OR1, OR0 = 00 : selected angular range = 10 bit over 360°, resolution = 0.35° per step ,
- ClampMdEN = 0 : DAC output voltage is $(0 - 100\%)*V_{ref} = (0 - 100\%)*1.2V$
- „FB_intEN“ = 0 : OPAMP is configured as current source with external 1x gain.

The resulting output current is proportional to the angle: $I_{out} = (0...100\%)*V_{ref} / R_E = 0...20mA$ from 0° to 360°

For this configuration, a buffer capacitor at pin VDD3V, a general purpose bipolar NPN transistor, one resistor for the current setting (R_E) and another filter capacitor for the emitter voltage are required. See Figure 7 for unused pin connections.

The complete circuit requires only 3 wires:VDD, VSS and Iout. The 1.2V reference may be taken from an external LDO or from the internal 3.3V regulator using a resistor voltage divider.

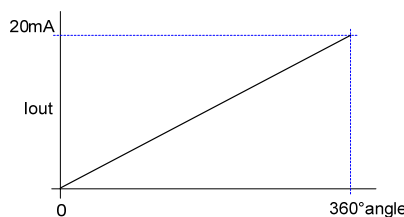
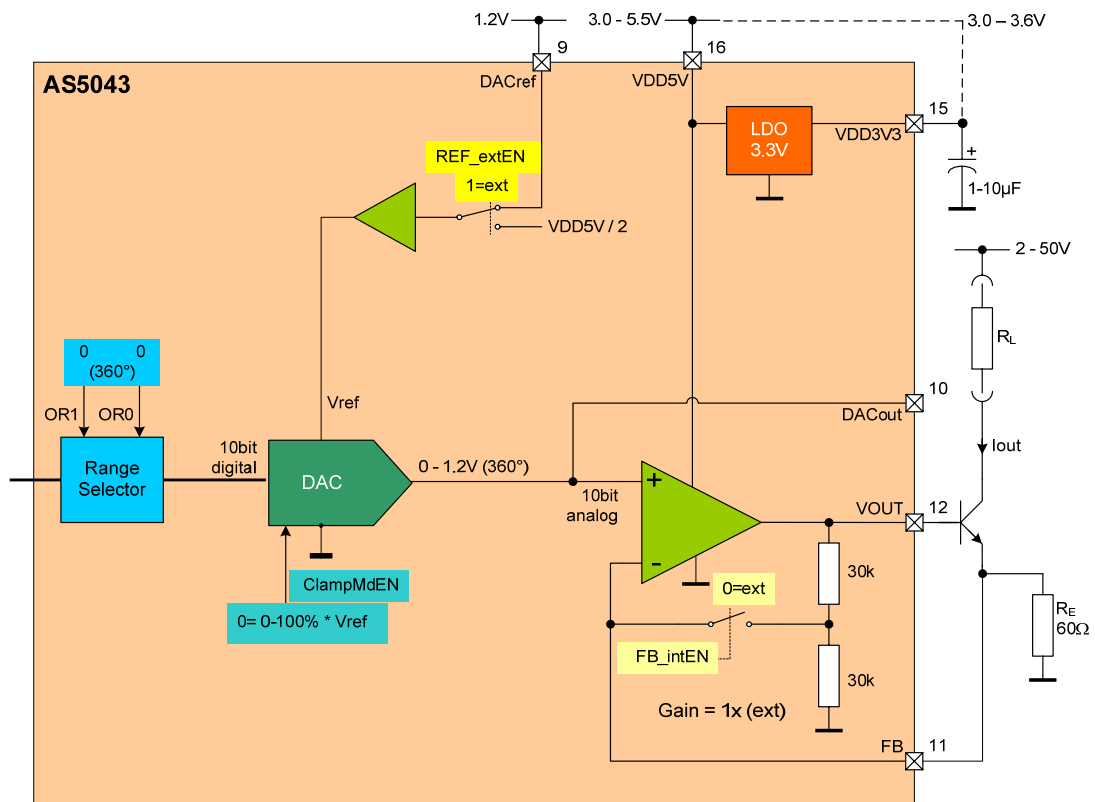


Figure 12: output configuration for current output

4.7 Application Example 7: reversed response curve

The output voltage versus angle response curve can be mirrored by setting the CCW bit in the OTP register to 1. Shown below is an example of a 0°-270° response curve, generated by an external gain of 2.66x in 360° mode and 3.3V supply voltage.

By default, the slope is rising from the digital 0000 position in clockwise direction (see Figure 13a). It reaches a maximum at 270° (digital position 768) and stays at VDD from 270° to 360°.

Setting the CCW bit in the OTP register (see Figure 5) reverses the response curve. The rising slope in clockwise direction becomes a falling slope (see Figure 13b).

Additionally, by shifting the zero position in the OTP register, the start of the falling slope can be shifted to the mechanical zero position (see Figure 13c). In this case, the value 256 is subtracted from the zero position in order to shift the zero position by -90°. The slope now starts with a maximum output voltage at 0° and reaches a minimum at 270°.

Note: A reversal of the response can be certainly applied to any curve in any mode. Placing the magnet at the bottom of the IC rather than at the top has the same effect as setting the CCW-bit to 1.

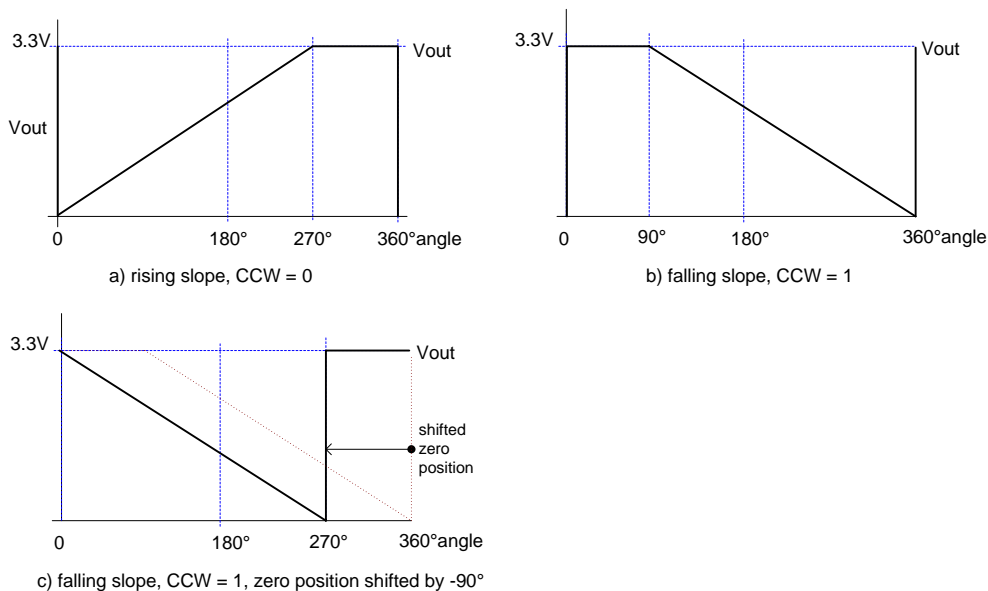


Figure 13: output response curve inversion with CCW bit

4.8 Application Example 8: Overvoltage and Reverse Polarity Protection

Figure 14 shows a method to add a high level overvoltage and reverse polarity protection for both supply and analog output using just a few external low cost components.

4.9 Overvoltage protection at supply:

This block consists of components Q1, Q2, D1, D2, R2..R5. While V_{in} is lower than ~6.5V, Q1 is fully on. Base current for Q1 is supported from R5. If V_{in} rises above ~6.5V, Zener diode D2 becomes conductive and draws base current into Q2. This transistor turns on and shuts Q1 off. Consequently the supply for the AS5043 is turned off. It will be automatically restored once V_{in} drops again below ~6.5V. The shutoff threshold can be adjusted by D2, R2 and R3. D1 is added for improved temperature stability of the circuit. R4 sets the slope of the shutoff level. The maximum allowed input voltage depends mainly on the maximum Collector-Emitter breakdown voltage of Q1 and the maximum Gate-Source voltage of Q3 (see 4.11).

4.10 Overvoltage protection at output pin

This is simply achieved by adding the series diode D4. The circuit can still provide up to 4.5V output voltage (using a schottky diode), as the feedback circuit R_f and R_g is connected after the diode. In case of overvoltage at the output, pin VOUT is protected by D4 and pin FB is protected by R_f and R_g . The maximum allowed overvoltage at the output depends on the Breakdown voltage of D4, which is usually very high (typ. 100V for BAT41) and the current into pin FB, which flows over the internal protection diode (shown in block diagram) to VDD5V. The current through the internal protection diode should be limited to ~1...10mA in case of overvoltage.

4.11 Reverse polarity at supply

This block consists of components Q3, R1 and C1. D3 is a parasitic diode inside Q3. Transistor Q3 must be an N-channel Enhancement MOSFET. In normal operation, Q3 is operating in reversed mode, with source and drain reversed (drain is more negative than source). However, since the gate voltage is positive with respect to source, Q3 is conducting and acts like a switch. In the reverse polarity case, Q3 is in normal mode (drain more positive than source), but the gate level is negative, causing Q3 to switch off. The maximum allowed reverse voltage is limited by the maximum negative gate-source voltage of Q3 (typ. +/-20V for BS170). For higher overvoltage protection and reverse polarity voltage levels, a resistor in parallel to C1 may be added, creating a voltage divider with R1. However, the divider must be designed such that Q3 gets enough gate-source voltage in normal 5V-operation to turn this transistor fully on.

R1 / C1 protect the gate from overvoltage spikes and overcurrent.

4.12 Reverse polarity at output

A reverse polarity at the output is again protected by Q3, as it remains switched off, since it does not get any positive gate-source voltage to turn on.

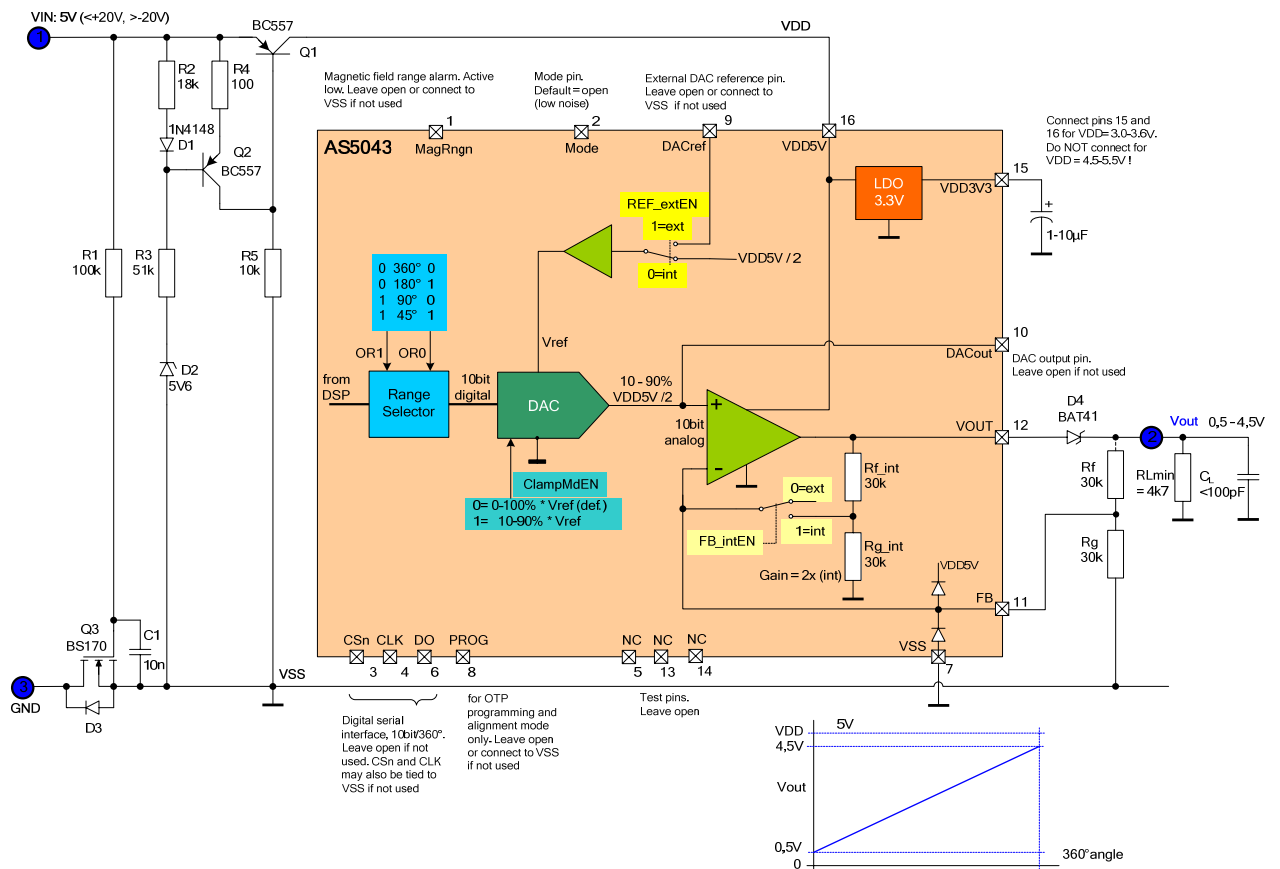
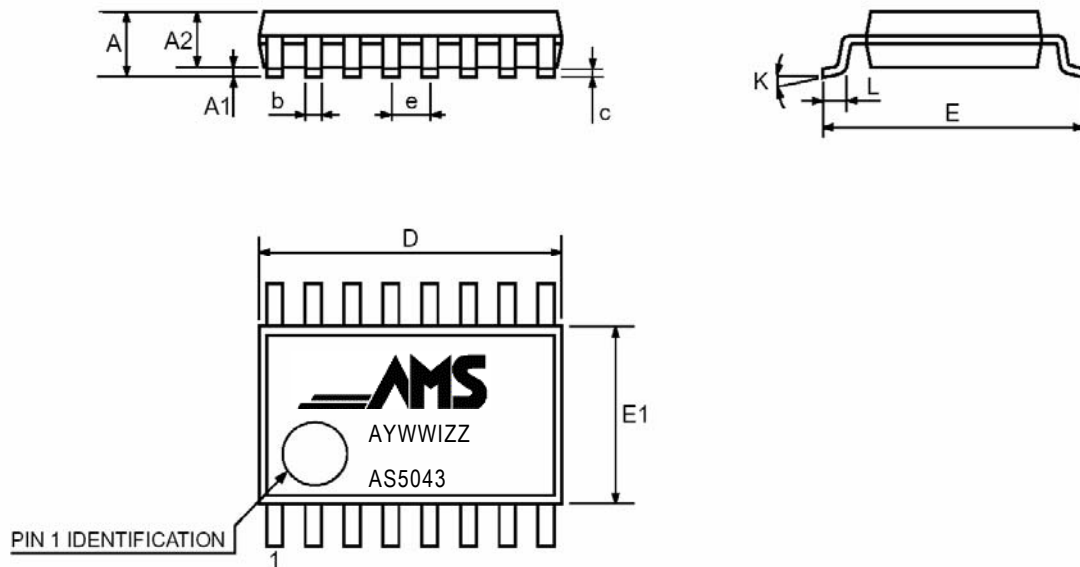


Figure 14: High level overvoltage and reverse polarity protection

5 Package Drawings and Markings

16-Lead Shrink Small Outline Package SSOP-16



Dimensions						
Symbol	mm			inch		
	Min	Typ	Max	Min	Typ	Max
A	1.73	1.86	1.99	.068	.073	.078
A1	0.05	0.13	0.21	.002	.005	.008
A2	1.68	1.73	1.78	.066	.068	.070
b	0.25	0.315	0.38	.010	.012	.015
c	0.09	-	0.20	.004	-	.008
D	6.07	6.20	6.33	.239	.244	.249
E	7.65	7.8	7.9	.301	.307	.311
E1	5.2	5.3	5.38	.205	.209	.212
e	0.65			.0256		
K	0°	-	8°	0°	-	8°
L	0.63	0.75	0.95	.025	.030	.037

1.1.1 Marking: AYWWIZZ

A: Pb-Free Identifier

Y: Last Digit of Manufacturing Year

WW: Manufacturing Week

I: Plant Identifier

ZZ: Traceability Code

JEDEC Package Outline Standard:

MO - 150 AC

Thermal Resistance $R_{th(j-a)}$:

79.4 K/W in still air

IC's marked with a white dot or the letters "ES" denote Engineering samples

6 Ordering Information

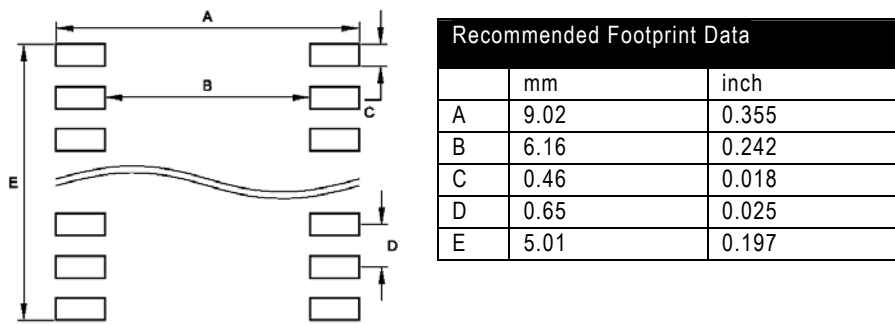
Delivery: Tape and Reel (1 reel = 2000 devices)

Tubes (1 box = 100 tubes á 77 devices)

Order # AS5043 for delivery in tubes

Order # AS5043TR for delivery in tape and reel

7 Recommended PCB Footprint:



8 Revision History

Revision	Date	Description
1.3	Sep.20,2006	Add Application Example 3: angular sub-range adjustment
1.2	Apr.14, 2006	Add Application Example 8: Overvoltage and Reverse Polarity Protection , Update Figure 6
1.1	Oct. 03, 2005	Update added features for Date Codes A534xx and higher: Clamping levels: 10%/90% VDD, default OPAMP gain = external, falling slope in 90°/45°-modes. Update thermal resistance of IC package.
1.0	May 19, 2005	initial revision

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