

AS3536

Digital Audio/Video Processor

Preliminary
Product
Brief

1 General Description

The AS3536 is austriamicrosystems' third generation mobile entertainment platform digital audio/video processor. Its highly flexible architecture allows single chip solutions for high performance power optimised audio and video products with minimum count of external components.

For video applications the integrated video decoder hardware will provide high efficient video decoding at very low clock rates and the speed of the system can be scaled to the actual demanded video decoder complexity and resolution. All video decoder features for H.263/ MPEG-4/H.264 and VC-1 are implemented in a dedicated video hardware accelerator for minimal power consumption.

Using low power deep submicron technology gives outstanding performance in terms of power consumption and utmost integration densities for embedded on-chip RAM and ROM areas.

The AS3536 is intended as a microcontroller chip including all digital function blocks necessary for a portable audio or video player. These function blocks include on-chip RAM and ROM memories, interface blocks for data transfer and storage like USB, IDE, NandFlash, MMC, SD, SDIO, CE-ATA.

Based on the ARM926-EJ with large on-chip instruction and data caches and integrated MMU, the system gives full support for all kinds of operating systems from simple RTOS implementations up to Symbian OS, micro Linux and Windows CE.

The AS3536 contains an ultra low power stereo audio codec. It allows playback in higher than CD quality and recording in FM quality. It has a variety of audio inputs and outputs to directly connect electret microphones, 16 /32 headsets and auxiliary signal sources via a 3-channel mixer.

Further the device offers advanced power management functions. All necessary ICs and peripherals in a Digital Audio Player are supplied by the included AFE. The AFE also contains a Li-Ion battery charger. The single supply voltage may vary from 2.7V to 5.5V.

The AFE has an independent 32kHz real time clock (RTC) on chip which allows a complete power down of the system CPU.

austriamicrosystems provides a total system solution reference design including all necessary software blocks for low level HW drivers, device IO functions and a dedicated reference application with common audio and video features.

2 Key Features

Basic System

ARM926-EJ RISC Controller

- 32/16 bit RISC architecture
- 16-bit Thumb instruction set
- ARMv5TEJ extended DSP instruction set and single cycle MAC
- Memory Management Unit
- Embedded ICE JTAG debug interface
- 16KB Instruction + 16KB Data Cache
- up to tbd MHz clock speed
- power consumption: 0.265 mW/MHz including caches at typical conditions
- 32/16 bit RISC architecture

Memory

- 512 KByte embedded SRAM connected to AHB1
- 160 KByte ROM (128KB bootrom + 32KB GF-table)
- 32 KByte embedded SRAM connected to AHB2 as buffer memory within AHB2 bus domain
- external memory controller supporting
 - support for 32 bit data width
 - synchronous/asynchronous SRAM/Flash interface
 - SDR DRAM (single data rate DRAM)
 - supports 2 static and 2 dynamic external memory devices
 - support three IO voltage levels: 1.8/2.5/3.3 V
 - pads with programmable drive strength
 - 133 MHz max external memory clock frequency



AMBA Bus

- two AHB bus segments
 - AHB1 with all Core/Memory high performance elements running up to 133 MHz
 - AHB2 with all peripheral interface blocks running at max. 66 MHz bus speed
- AHB bus bridge between AHB1 and AHB2
 - synchronous 1:1 mode
 - asynchronous mode
- AHB interconnect matrix for high throughput
 - AHB to APB bridge
 - connected to AHB2

DMA controller

One DMA controller located in each of AHB1 and AHB2 bus domain

- DMA1 in AHB1 bus domain
 - 8 simultaneously opened DMA channels
 - 16 DMA requests
- DMA2 in AHB2 bus domain
 - 8 simultaneously opened DMA channels
 - 32 DMA requests

Interrupt Controller (VIC)

Two vectored interrupt controllers, one in each bus domain.

- Support for 32 non-vectored interrupts
- Support for 32 vectored interrupts

PWM outputs

- four PWM output channels
- each channel can run independently or synchronized
- period, pulse width and phase defined by 8-bit registers (phase only in synchronized mode)
- two independent rotary decoders with programmable glitch filter
- programmable count direction
- programmable interrupt on zero count
- zero count can stop PWM modulators

Timer and Watchdog

- two independent timer blocks (A+B) with two 32 bit counters each
- two timer trigger event inputs
- watchdog

Chip Control Unit

- two independent 1 GHz PLL generators (PLLA, PLLB)
 - 24 MHz crystal oscillator
 - optional usage of external oscillator
 - four programmable clock outputs
- n chip version number
- control of IO multiplexing
 - universal spare registers
 - clock gating / block enables
 - JTAG disable bit

Keyscan Controller

- configurable 1x4 to 4x4 matrix
- low power mode
- interrupt generation

IMON

- Intelligent hardware monitor for bus and system profiling for continuous system monitoring and power optimisation.
- very flexible selection of input events
- monitoring averaging or peak conditions
- scalable counters
- programmable interrupt generation

OTP

- 256 Bit one-time-programmable memory
- n contains unique ID

Interfaces

Audio Interface

I2S input interface

- FiFo (32x48) buffered
- DMA support
- 24 bit mode
- SPDIF input bridge

I2S output interface

- FiFo (128x48) buffered
- DMA support
- 16/18/24 bit modes
- SPDIF output bridge

synchronous I2SIN to I2SOUT streaming mode

USB 2.0 HS & OTG Interface

- Up to 480Mbit/s transfer speed
- USB 2.0 HS/FS physical including OTG support
- USB 2.0 HS/FS digital core including OTG host
- Dedicated dual port buffer RAM
- DMA bus master functionality
- total of seven endpoints (1xCONTROL, 3xIN, 3xOUT)

IDE Host Controller

- Supporting Ultra ATA 33/66/100 modes
- Programmable IO and Multi-word DMA capability
- Dedicated dual port buffer RAM
- DMA bus master functionality

NandFlash Interface

- 8 and 16 bit flash support
- 3, 4 & 5 byte address support
- DMA support
- Basic hardware ECC for SLC
- extended BCH error correction for MLC (correction of 4 / 8 / 16 errors within 512 byte)
- caching of ECC data for 2K/4K/8K page sizes to write ECC data to spare region

MMC/SD Interface

- Mobile Storage controller supporting various standards
 - SD card according to SD Phys. Layer Spec V2.0
 - SDHC card according to SD Phys. Layer Spec V2.0
 - SDIO interface according to SD spec part E1, SDIO Spec V2.0
 - Multimedia Card according to MMC Spec V4.2 including MMCplus and MMC Mobile
 - Consumer Electronics Advanced Transport Architecture (CE-ATA version 1.2)
- Other Features
 - Integrated 2048 byte FiFo
 - Separate clock for bus interface and card interface
 - 1, 4 or 8 bit data width for MMC card IF
 - 1, 4 bit data width for SD card IF
 - AMBA AHB bus interface

Memory Stick Interface

- Memory Stick and Memory Stick Pro support
- 20 MHz serial, 40 MHz parallel clock

Synchronous Serial Interface

- two independent SSI interfaces
- Master/slave
- TX/RX FiFo buffering (16 byte)
- DMA support
- 8/16 bit support

2-wire Control Interface

- I2C interface
- master/slave function
- FiFo buffering (16 byte)
- DMA support
- max. 400 KHz speed

UART

- baud rates up to 2 Mbit/s
- internal RX/TX FiFo buffering (64 byte)
- DMA support
- Irda SIR Encoder/Decoder

General Purpose IO

- most of the PINs configurable as GPIO
- configurable drive strength
- configurable pull-down function
- each GPIO PIN can be used as programmable interrupt source

Generic Infrared Interface

- modulated or digital transmit and receive
- independent transmit and receive FiFo buffers (16 entries each)
- direct interrupts for transmit and receive FiFo level monitoring

XM Satellite ready

- integrated XM DT interface
- LVDS interface
- Uses internal PLLB for generation of 45.1584 MHz clock

Display Interface

Two display output interfaces are available: either DBOP for simple small resolution displays or full RGB/LCD controller IF for high resolution displays

DBOP

- configurable interface for different types of uController
- system interfaces (Intel 80xx or Motorola 68xx style)
- FiFo buffer (128x32) and DMA support
- 8 or 16 bit modes

LCD Controller

- FiFo input data buffer (dual 16x64)
- supports single and dual panel mono STN
- supports single and dual panel color STN
- supports TFT color displays
- wide range of programmable resolutions: 320x200, 320x240, 640x200, 640x240, 640x480, 800x600, 1024x768
- 1/2/4/8 bpp palettized color for STN or TFT
- 16 bpp true color STN or TFT mode
- 24 bpp true color TFT
- TFT modes with 12 bpp direct 4:4:4 RGB, 16 bpp direct 5:5:5, 16bpp direct 6:6:6 and 16bpp direct 5:6:5 both with common intensity bit), 24 bpp direct 8:8:8
- hardware cursor support for single panel displays
- programmable parameters for all key parameters (frequency, timings, resolution, bpp, color modes, ...)

Video Output

CCIR-656 compatible pixel output port to support an external PAL/NTSC video encoder.

- 27 MHz data rate
- 8 bit parallel data IF with YCrCb 4:2:2 encoding

Audio Engine

Audio Accelerator

- Ultra low power accelerator for decoding of MP3, WMA and AAC.
- includes ten-band equalizer with 64 steps (-20 ÷ 20 db gain) and 32-step volume control

MP3 features

- 9 MHz clock frequency for MP3 decoding with 320 kbit/s input bit rate / 48 KHz audio sampling rate
- support MPEG-1 layer III and MPEG-2 layer III (ISO11172-3 and ISO13818-3) formats
- support for constant and variable bit rate from 8 to 320 kbps

WMA features

- WMA V8 and V9 compatible WMA decoder
- support of bit rates from 5kbps up to 382 kbps

AAC features

- AAC LC
- AAC main profile
- support of VBR

Audio Post-Processor

For flexible audio signal processing an internal audio matrix is available together with a audio mixer, equalizer and sample rate converter.

- 5 band graphic equalizer
- I2SIN input sample rate conversion for audio mixing with signals running on other sampling rate
- audio mute
- L/R channel swap
- gain attenuation
- limiter modes

Security Engine

- AES ciphering supporting 128 bit keys with ECB, CBC and CTR block cipher modes
- DES and 3-DES ciphering supporting ECB and CBC block cipher modes
- RC-4 ciphering supporting 40 bit and 128 bit key expansion modes
- All cipher modes support both encrypt and decrypt operations
- SHA-1 and MD-5 hashing algorithm with support for HMAC mode (key sizes of 1 to 64 byte)
- power optimized True Random Number Generator (TRNG) supporting initial seeding and 32 bit random word every 128 clock cycles

Video Engine

The video engine consists of a video accelerator and of an independent video postprocessor. Features of the video postprocessor can be used independently of the chosen video decoding algorithm (running either in the video accelerator or in software).

- Minimum power consumption of HW video engine
- < 18mW for H.264 PAL/NTSC resolution
- Video Accelerator
- MPEG 4 simple profile, Levels 0 - 5
- H.263 profile 0, Levels 10 - 70
- H.264 / AVC Baseline, Levels 1 - 3.1
- VC-1 (Windows Media Video 9) main profile, levels Low, Mid and High
- JPEG Baseline DCT, sequential
- Video resolutions (for MPEG-4/H.263/H.264/VC-1)
 - up to 720x576 at 25 fps (PAL/DVD) or
 - up to 720x480 at 30fps (NTSC)
- ultra low CPU load < 3MHz

Video Post-Processor

- Integrated colour space conversion YCbCr to RGB
- Proprietary scaling algorithms for better quality on handset resolutions
- image rotation
- cropping function for viewing large images on small displays in original size
- masking feature for easy user interface implementation
- alpha blending support for two variable sized regions
- picture-in-picture support

Extended system features

Boot Options

The chip contains an on-chip ROM Bootloader that supports booting from various kinds of external flash devices. During boot, the application firmware is loaded from the external flash device into the RAM. In addition to this boot functionality, also the firmware programming and firmware update is supported.

- SLC or MLC NandFlash
- static Flash (MPMC)
- serial NOR Flash
- IDE
- SD interface NandFlash
- eMMC interface NandFlash
- Bootloader concept with 1st/2nd level loader for initial firmware programming and firmware update
- secured firmware update mechanism
- optional support of hash authentication or firmware encryption

Modes of operation

- Normal operation
- Hibernation mode (clock stopped)

Audio Frontend Features

Audio Features

- Audio power consumption:
 - 5mW: 96dB DAC to Headphone @ 1.8V, 32
 - 7mW: 100dB DAC to Headphone @ 2.9V, 32
- n Sigma Delta DAC
 - 96dB SNR ('A' weighted) @ 1.8V
 - 100dB SNR ('A' weighted) @ 2.9V
 - 8-48kHz sampling frequency
- Sigma Delta ADC
 - 83dB SNR ('A' weighted) @ 1.8V
 - 8-24kHz sampling frequency
- Microphone Input
 - 3 gain pre-setting (28dB/34dB/40dB) and AGC
 - 32 gain steps @1.5dB and MUTE
 - supply for electret microphone
 - microphone detection
 - remote control by switch
- Line Input
 - volume control via serial interface
 - 32 steps @1.5dB and MUTE
 - stereo or 2x mono
- Audio Mixer
 - 6 channel input/output mixer with AGC
 - mixes line inputs and microphones with DAC
 - left and right channels independent
- Line Output
 - volume control via serial interface
 - 32 steps @1.5dB and MUTE
 - 1Vp @10k
 - ground noise cancellation
- High Efficiency Headphone Amplifier
 - volume control via serial interface
 - 32 steps @1.5dB and MUTE
 - 2x12mW @16 driver capability@ 1.8V supply
 - THD -74dB @16 ; 1.8V
 - 2x40mW @16 driver capability@ 2.9V supply
 - THD -77dB @16 ; 2.9V
 - headphone and over-current detection
 - phantom ground eliminates large capacitors
 - ground noise cancellation

Power Management

- Voltage Generation
 - step down for CPU core (1.2V typ, 250mA)
 - step down for peripheral (0.65V-3.4V, 250mA)
 - LDO1 for AFE audio supply (1.7V, 50mA)
 - LDO2 for AFE IO/audio supply (2.7V, 200mA)
 - LDO3 for peripherals (1.2V-3.5V, 100/200mA)
 - LDO4 for peripherals (1.2V-3.5V, 100/200mA)
 - VBUS comparator
 - separate input for LDO3
 - power supply supervision
 - 5sec and 10sec emergency shut-down
- Backlight Driver
 - step up for backlight (15V (25V))
 - current control mode (1.1-36mA)
 - voltage control mode
 - automatic dimming
 - over-voltage protection
- Battery Charger
 - automatic trickle charge (55mA)
 - prog. constant current charging (55-460mA)
 - prog. constant voltage charging (3.9V-4.25V)
 - current limitation for USB mode
 - integrated battery switch

General AFE Features

- Supervisor
 - automatic battery monitoring with interrupt generation and selectable warning level
 - automatic temperature monitoring with interrupt generation and selectable warning and shutdown levels
- Real Time Clock
 - ultra low power 32kHz oscillator
 - 32bit RTC sec counter, 96 days auto wake-up
 - selectable alarm (seconds or minutes)
 - 128bit free SRAM for random settings
 - 32kHz clock output to peripheral
 - voltage generation
 - trimable oscillator
 - <1uA total power consumption
- General Purpose ADC
 - 10bit resolution
 - 19 inputs analog multiplexer
- Interfaces
 - 2 wire serial control interface
 - reset pin with selectable delay, power good pin
 - 64bit unique ID (OTP)
 - 23 different interrupts

Power Consumption

Playback use case: MP3 / AAC / WMA playback 128kbit/s, 44.1 KHz, output level 150 mVrms, no external memory. Depending on output quality, following power consumption values are achieved.

Standby use case: clock stopped, only voltage generation for keeping memory content is on, system will wakeup by timer interrupt..

Table 1. power consumption

Audio Playback, 100 dB SNR	16.5 mW
Audio Playback, 94 dB SNR	14.1 mW
Audio Playback, 92 dB SNR (1)	10.6 mW
H.264 Video Decode QVGA (2)	56 mW
H.264 Video Decode D1 (2)	120 mW
Standby	1.4 mW

Notes

(1) Class-D Headphone output amplifier

(2) System power consumption, includes power consumption for external mobile SDRAM memory. Display and display backlight power consumption is not included.

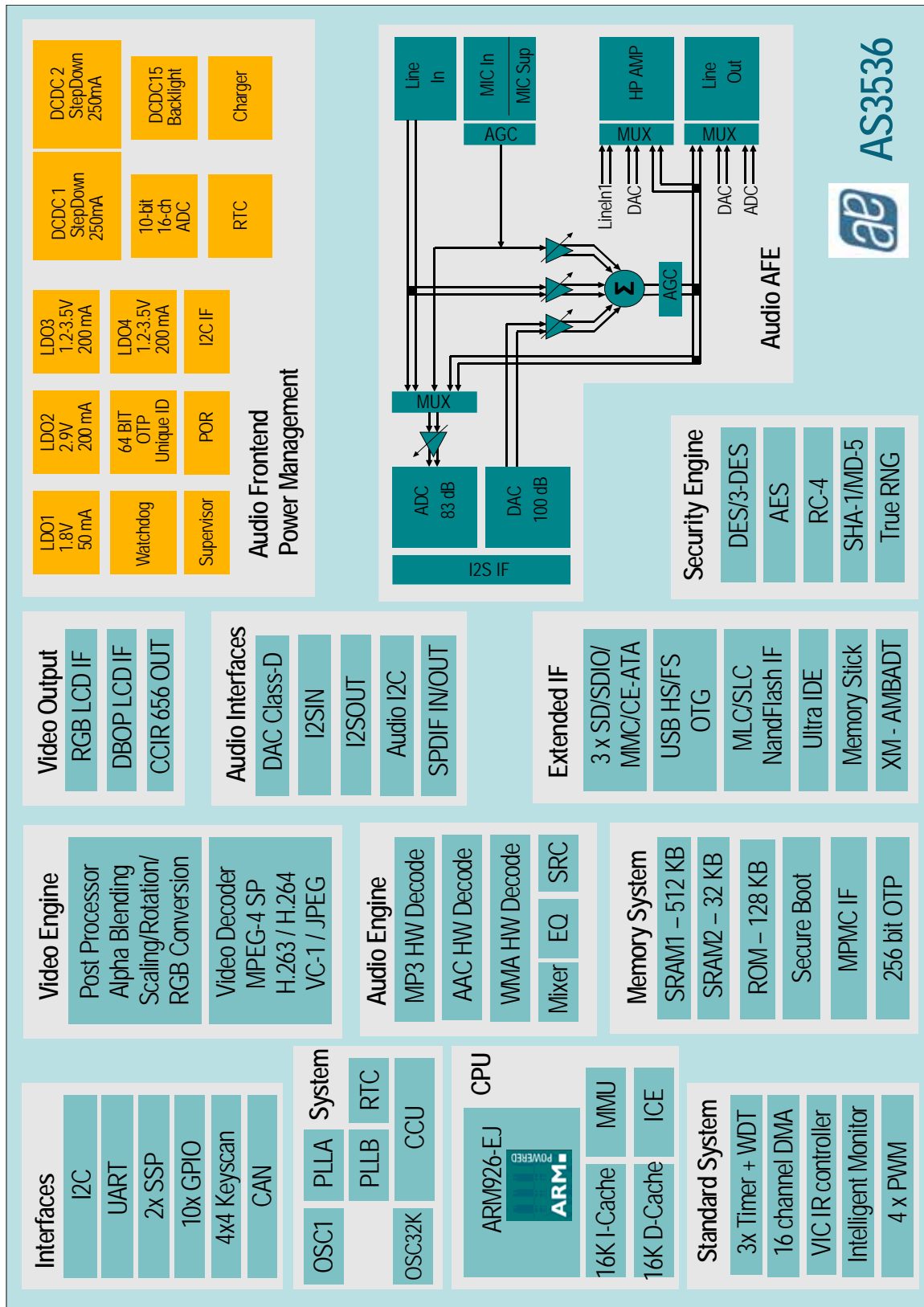
Packaging

Single chip CTBGA 10x10 mm with 0.5 mm ball pitch, 244 Balls.

3 Application

Portable Multimedia Players with ultra low power consumption.

Figure 1. AS3536 Block Diagram



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