HIGH VOLTAGE CMOS TECHNOLOGIES
FOR ROBUST SYSTEM-ON-CHIP DESIGN

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In the past Smart Power System-on-Chip (SoC) products were almost exclusively designed on Bipolar-CMOS-DMOS (BCD) technologies. These products address applications as diverse as power management for mobile phones, motor drivers, printer head drivers, automotive bus transceivers and dataline drivers for high speed internet or Voice over IP (VoIP). The trend towards SoC design for lowering form factor and system cost has favored the use of low cost CMOS processes. High Voltage CMOS (HV-CMOS) processes have started to replace BCD processes in some applications that were previously dominated by BCD technologies. LCD display driver ICs supporting voltages up to 40V were the first large volume application for HV-CMOS processes. Other applications such as power management, bus transceivers, printer head drivers will soon employ HV-CMOS technologies. This is driven by HV-CMOS process and device architecture advances as well as progress in circuit modeling, Process Design Kits (PDKs), ESD structures and device reliability. HV-CMOS technologies have begun to offer designers equivalent functionality compared to typical BCD technologies without the additional process complexity. The modular HV-CMOS process architecture also offers easier scalability towards smaller geometries and straight-forward integration of embedded memories. The tradeoff is increased complexity of HV device layouts and PDK components.

HV-CMOS PROCESS ADVANCES

Recent publications have demonstrated HV-CMOS processes scaled down to feature sizes as low as 0.13µm [1]. By adding two implant mask levels to the core CMOS process for implementing 20V HV devices, the needs of applications such as power management for mobile handsets can be served. The performance and size of high voltage devices is determined by the specific on-resistance at a given voltage rating. HV-CMOS can meet the best reported values for BCD processes [2]. An increasing number of other applications previously reserved for BCD technologies such as printer head drivers and automotive bus transceivers can now be addressed by using HV-CMOS. Figure 1 shows a 0.35µm HV-CMOS FlexRay transceiver [3] with a voltage rating of +/-58V and ESD capability of +/-4kV HBM (Human Body Model). This product was designed on an HV-CMOS technology requiring the addition of only two mask levels to the core CMOS process.
Such high-performance HV-CMOS process architectures have been enabled by the use of predictive computer simulation (TCAD) [4] of HV-CMOS devices. Performance and reliability can be optimized by tailoring dopant distributions and device layouts while maintaining the lower cost of CMOS processes.

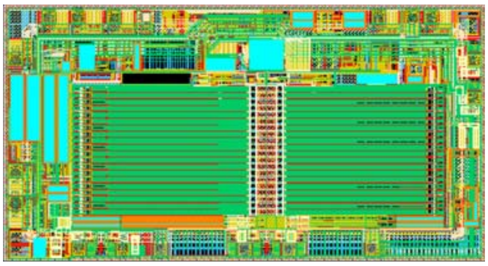

Figure 1: FlexRay bus transceiver manufactured in 0.35µm HV-CMOS [3].

HV-CMOS PDK

Current HV-CMOS Process Design Kits (PDKs) offer a variety of design rule verification routines for ESD and latch-up which enable robust High-Voltage designs. This is accomplished without the additional process complexity of buried layers used in BCD processes [5]. The use of scalable SPICE models and parameterized cells (Pcells) both for core CMOS and HV devices is a standard feature in modern HV-CMOS PDKs. Some foundries and third party service providers offer PDKs which include a complete "plug and play" set-up for HV-CMOS processes. The FSA Mixed-Signal/RF Subcommittee has developed mixed-signal/RF PDK and SPICE model checklists which gives an overview on the contents required to ensure PDK quality. Such high quality PDKs include all the components for a complex mixed-signal design including the additional functionality to address the HV requirements. A representative HV-CMOS Design Flow is shown in Figure 2.

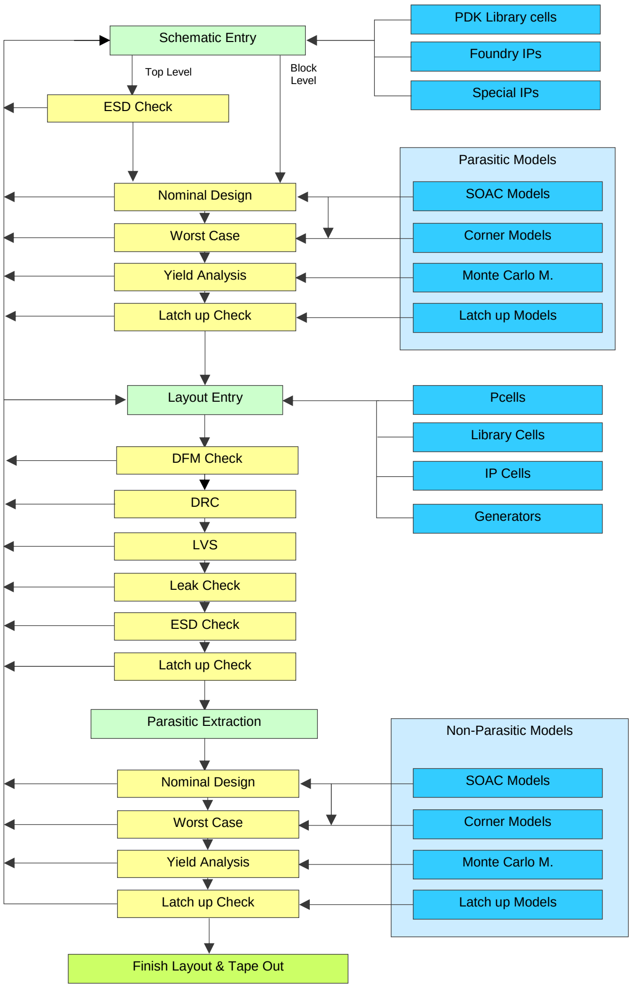

Figure 2: HV-CMOS Design Flow

HV-CMOS MODELING

Highly accurate compact modeling is essential for any analog/HV IC design. This is especially true for HV-CMOS technologies. The behavior of a HV MOS transistor is generally different compared to standard analog low voltage MOS transistors. Increased breakdown voltages are achieved by an additional “drift region” between the gate and drain terminal. This HV MOS device type is called Lateral Diffused MOS (LDMOS) transistor. The lack of existing analytical compact models in commonly available simulators for scalable LDMOS transistors requires the introduction of sub-circuits. The LDMOS transistor sub-circuits need to be compatible with all major SPICE simulators and should include certain physical effects; scalable quasi-saturation effects, the lateral channel doping gradients, self-heating effects, substrate currents as well as parasitic capacitances and diodes.

With this approach, highly accurate LDMOS SPICE models can be generated from standard BSIM3v3 or EKV low voltage transistor models.
Comprehensive 1/f noise and mismatch modeling for the full set of low voltage and high voltage MOS devices as a function of geometry, threshold voltage and on–resistance builds the basis for robust designs in HV-CMOS processes. Automotive designs often require an extension of circuit model verification for temperatures ranging from 150°C to 200°C.

Accurate statistical modeling is a key element of Design for Yield (DFY) [6]. Statistical SPICE models (Monte Carlo and Corner) describe the process variation of high voltage transistors and are derived from the multi-dimensional distribution of relevant production control parameters. Such improved modeling using statistical corners instead of traditional worst case vectors enables a minimum 10% reduction in chip area and reduced power consumption for HV-CMOS ICs. Monte Carlo simulation models including global and local variations (mismatch) are another essential part of a HV-CMOS PDK. These methods enable simulation-based yield optimization in customer designs and high voltage IP blocks provided by the foundry.

Due to the absence of buried layers in HV-CMOS processes designers must be provided with accurate and complete substrate current models. This is achieved by providing HV MOS transistor models that include all parasitic bipolars in the lateral and vertical directions (Figure 3). A typical sub-circuit includes two SPICE Gummel Poon models representing the parasitic bipolar devices including geometry scalable prediction of parasitic substrate currents.

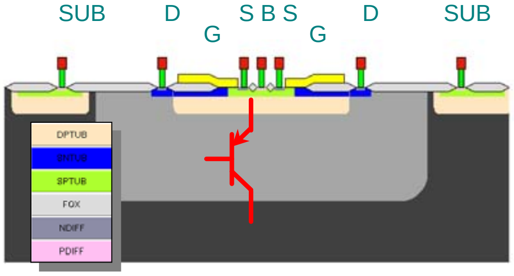

Figure 3: HV-CMOS transistor with the parasitic bipolar transistor.

MEETING TRANSISTOR LIFETIME REQUIREMENTS

In order to guarantee compliance with quality standards such as JEDEC, a variety of accelerated lifetime tests such as electro-migration, hot carrier injection (HCI) and threshold voltage shift (NBTI) must be performed. Qualification test results lead to the specification of a certain Safe Operating Area (SOA) for each device. Designers must ensure that all low voltage and high voltage devices are operating within the SOA for the lifetime of the product.
Only a very small number of devices can be controlled manually.

Therefore an automated Safe Operation Area verification routine (SOA) is essential for ensuring a robust HV-CMOS design. The SOA verification routine should be configurable to allow its use in all simulations performed during the design phase. A reliable SOA verification routine not only has to check for dynamic limitations such as hot-carrier effects, but also for other limitations including punch-through and the correct biasing of diodes.

PARASITIC EFFECTS

The switching of inductive loads can result in the turn-on of parasitic devices. A diode biased in the forward direction will result in current injection into the substrate and the possibility of latch-up. Using accurate models of all parasitic devices, the HV-CMOS designer can now detect latch-up critical configurations at the schematic level. Therefore a latch-up verification routine is then conducted during top-level simulation. The latch-up verification routine evaluates all injected substrate currents and suggests additional constraints for the layout. The latch-up verification routine can, for example, suggest changes in the spacing between critical devices or the addition of deep n-well guard rings.

PHYSICAL VERIFICATION AND DESIGN FOR MANUFACTURABILITY

During the layout verification phase, additional Design Rule Check (DRC) and Layout Versus Schematic (LVS) functionality is required to account for the various operating voltages (20V to 120V) used in System-on-Chip product designs [3]. For supply voltages above 50V the effect of parasitic field transistors must be taken into account. These parasitic field transistors can result in leakage current between isolated areas. This issue is addressed by an additional Leakage verification routine as part of the HV-CMOS PDK.

Yield and reliability issues not covered by DRC can be addressed by Design For Manufacturability (DFM) verification routines. This includes automatic placement of power metal fill patterns and optimization of the number and placement of contacts and vias for HV driver transistors.

HV-CMOS ESD

Electrostatic Discharge (ESD) robustness is a critical part of any High Voltage technology. As opposed to BCD processes which typically use buried layers as part of the ESD structures, the HV-CMOS processes rely on the available wells and more sophisticated ESD structure layouts. The development of HV ESD structures has been facilitated by progress in predictive TCAD [4]. With these measures equivalent ESD robustness can be achieved for HV-CMOS processes [3] as compared to BCD processes, even though there may be a penalty in the size of ESD structures in some cases. In most cases, the larger ESD structures for HV-CMOS are negligible in their overall contribution to chip size in an HV SoC product design.
Irrespective of the choice of technology (HV-CMOS vs. BCD), a comprehensive and thorough ESD design flow is important to achieve ESD robustness early in the design phase. This includes a product-related ESD protection concept which is supported by a library of silicon-proven ESD protection cells as part of the PDK. Additionally, an ESD check at the schematic level and at the layout level must be available in the PDK in order to verify ESD capability is maintained throughout the complete design phase. As robust ESD design to some extent is still based on human experience some foundries offer special ESD review services to ensure first-time-right designs.

CONCLUSION

Based on progress in process and device architecture as well as PDK functionality, HV-CMOS can increasingly address applications that were previously reserved for more complex BCD processes.

Robust HV design still depends on the skill of the design team. Sophisticated “plug and play” HV-CMOS PDKs can however make the life of the design team much easier. Utilities such as SOA, Leakage, ESD and Latchup verification routines included as an integral part of a HV-CMOS PDK enable first-time-right designs. Some foundries further support this by offering additional ESD and DFM services and design reviews.

References

[1]C.Grelu et al., Proceedings of the 2005 International Symposium on Power Semiconductor Devices & ICs, Santa Barbara CA.

[2] S.Pendharkar et al. Proceedings of the 2004 International Symposium on Power Semiconductor Devices & ICs, Kitakyushu JP.

[3]F.Baronti et al., Proceedings of the Design Automation and Test conference 2006 (DATE06).

[4]R.Minixhofer et al., Proceedings European Simulation Symposium (ESS), Dresden(Germany),October 23–26 2002.

[5] http://www.austriamicrosystems.com/05foundry/environment_start.htm

[6] Norman J. Rohrer, Introduction for Statistical Variation and Techniques for Design Optimization, Tutorial, ISSCC 2006.

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