

Model Notes AS8221

1 Model Overview

1.1 Implemented functionalities

- Device status management (Normal, Receive Only, Standby, Go to Sleep, Sleep, Power Off)
- Supply voltage monitor
- Read-out capability
- Temperature monitor
- Local and remote wake-up
- Transmitting and Receiving
- Bus-error and state flags
- Signal timings
- Thermal behavior
- Debug mode for internal state machine

1.2 Parameters

- | | | |
|------------------|---------------------|--|
| ▪ r_open | (default = 1.0e6) | off resistance of inner switches [Ohm] |
| ▪ r_closed | (default = 1.0e-3) | on resistance of inner switches [Ohm] |
| ▪ rise_time | (default = 10.0e-9) | switching rise time [s] |
| ▪ fall_time | (default = 10.0e-9) | switching fall time [s] |
| ▪ v_BGE_H_ratio | (default = 0.7) | BGE high level input voltage (ratio of Vio) |
| ▪ v_BGE_L_ratio | (default = 0.3) | BGE low level input voltage (ratio of Vio) |
| ▪ v_RxEN_H | (default = 4.0) | RxEN high level output voltage [V] |
| ▪ v_RxEN_L | (default = 0.4) | RxEN low level output voltage [V] |
| ▪ v_TxD_H_ratio | (default = 0.7) | TxD high level input voltage (ratio of Vio) |
| ▪ v_TxD_L_ratio | (default = 0.3) | TxD low level input voltage (ratio of Vio) |
| ▪ v_TxEN_H_ratio | (default = 0.7) | TxEN high level input voltage (ratio of Vio) |
| ▪ v_TxEN_L_ratio | (default = 0.3) | TxEN low level input voltage (ratio of Vio) |
| ▪ v_RxD_H | (default = 4.0) | RxD high level output voltage [V] |
| ▪ v_RxD_L | (default = 0.4) | RxD low level output voltage [V] |
| ▪ t_sleep | (default = 40.0e-6) | timeout from go-to-sleep to sleep mode [s] |
| ▪ t_TxEN_timeout | (default = 2.0e-3) | timeout for asserted TxEN [s] |
| ▪ v_STBN_H_ratio | (default = 0.7) | STBN high level input voltage (ratio of Vio) |
| ▪ v_STBN_L_ratio | (default = 0.3) | STBN low level input voltage (ratio of Vio) |
| ▪ v_EN_H_ratio | (default = 0.7) | EN high level input voltage (ratio of Vio) |
| ▪ v_EN_L_ratio | (default = 0.3) | EN low level input voltage (ratio of Vio) |
| ▪ v_ERRN_H | (default = 4.0) | ERRN high level output voltage [V] |

▪ v_ERRN_L	(default = 0.4)	ERRN low level output voltage [V]
▪ t_ro_en_timeout	(default = 50.0e-6)	read-out enable timeout [s]
▪ t_ro_prop_errn	(default = 100.0e-9)	propagation delay EN -> ERRN [s]
▪ OT_th_H	(default = 165.0)	over-temperature high threshold [°C]
▪ OT_th_L	(default = 150.0)	over-temperature low threshold [°C]
▪ v_BAT_th_H	(default = 4.5)	V_BAT under-voltage recovery threshold [V]
▪ v_BAT_th_L	(default = 3.5)	V_BAT under-voltage detection threshold [V]
▪ v_CC_th_H	(default = 4.0)	V_CC under-voltage recovery threshold [V]
▪ v_CC_th_L	(default = 3.0)	V_CC under-voltage detection threshold [V]
▪ v_IO_th_H	(default = 1.6)	V_IO under-voltage recovery threshold [V]
▪ v_IO_th_L	(default = 1.1)	V_IO under-voltage detection threshold [V]
▪ t_uv_detect	(default = 0.4)	under-voltage detection time [s]
▪ t_uv_recover	(default = 0.4)	under-voltage recovery detection time [s]
▪ v_bus_active_h	(default = 225.0e-3)	bus activity detection high threshold [V]
▪ v_bus_active_l	(default = -225.0e-3)	bus activity detection low threshold [V]
▪ t_bus_activity_detect	(default = 200.0e-9)	bus activity detection time [s]
▪ t_bus_idle_detect	(default = 100.0e-9)	bus idle detection time [s]
▪ v_data0	(default = -225.0e-3)	data "0" detection threshold [V]
▪ v_data1	(default = 225.0e-3)	data "1" detection threshold [V]
▪ t_bus_RxD_01	(default = 40.0e-9)	delay from bus to RxD (0->1) [s]
▪ t_bus_RxD_10	(default = 40.0e-9)	delay from bus to RxD (1->0) [s]
▪ i_limit	(default = 100.0e-3)	bus current limit [A]
▪ t_BUS_ERROR	(default = 20.0e-9)	bus error detection time [s]
▪ i_BP_th_L	(default = 5.0e-3)	BP current lower threshold [A]
▪ i_BP_th_H	(default = 40.0e-3)	BP current higher threshold [A]
▪ i_BM_th_L	(default = 5.0e-3)	BM current lower threshold [A]
▪ i_BM_th_H	(default = 40.0e-3)	BM current higher threshold [A]
▪ v_diff_active	(default = 225.0e-3)	bus differential min active voltage [V]
▪ Vbat_wake_min	(default = 4.0)	min battery voltage for enabling wake-up [V]
▪ t_BWU_0	(default = 4.0e-6)	(bus wake-up) symbol "0" min hold time [s]
▪ t_BWU_1	(default = 4.0e-6)	(bus wake-up) symbol "1" min hold time [s]
▪ t_BWU_timeout	(default = 48.0e-6)	(bus wake-up) wake sequence timeout [s]
▪ v_WU_1	(default = 300.0e-3)	(bus wake-up) symbol "1" min bus voltage [V]
▪ v_WU_0	(default = -300.0e-3)	(bus wake-up) symbol "0" max bus voltage [V]
▪ v_LWU_thr	(default = 3.0)	(local wake-up) WAKE threshold voltage [V]
▪ t_LWU_filter	(default = 10.0e-6)	(local wake-up) filtering/hold time [s]
▪ instance_nr	(default = 1)	
▪ debug_flag	(default = false)	

1.3 Ports

▪ GND	electrical reference for the whole device
▪ BAT	supply pin (Vbat)
▪ CC	supply pin (Vcc)
▪ IO	supply pin (Vio)
▪ WAKE	local wake-up pin
▪ BP	"bus plus", positive bus wire
▪ BM	"bus minus", negative bus wire

- STBN "stand-by-not", host command pin
- EN "enable", host command pin
- ERRN "error-not", error indicator and read-out interface pin
- RxD "received data", received data interface pin
- TxD "transmit data", transmit data interface pin
- TxEN "transmit enable", transmit operation enable pin
- BGE "bus guardian enable", bus guardian enable pin
- RxEN "received enable", receive operation indicator pin
- INH1 "inhibit 1", device status indicator pin
- INH2 "inhibit 2", device status indicator pin
- t_case case temperature thermal pin

2 Supported Simulation Tools

Vendor	Simulation Tool	Version	Model Name	Availability
Cadence Design Systems	Virtuoso AMS Designer Simulator	5.1.41	AS8221_CAD_5.1.41_V1.0.zip	✓
Mentor Graphics	ADVance MS	2006.2a	AS8221_MGAD_2006.2a_V1.0.zip	on request
Mentor Graphics	SystemVision	5.0	AS8221_MGSV_5.0_V1.0.zip	✓
Synopsys Inc.	Saber HDL	2007.12	AS8221_SI_2007.12_V1.0.zip	✓

3 Installation

3.1 Virtuoso AMS Designer Simulator (5.1.41)

3.1.1 Library preparation

- Create a temporary folder and copy the file "AS8221_CAD_5.1.41_V1.0.zip" into this folder
- Unzip "AS8221_CAD_5.1.41_V1.0.zip"
- Create a folder within your simulation environment for the AS8221 simulation model library
- Move "inca.lnx86.157.pak" and ".inca.db.157.lnx86" into this folder

3.1.2 Library integration

- Modify "cds.lib":
 - Add new logical library: "as8221"
 - Add new physical library folder (your previous definition)
- Unpack library "as8221"
- Start your library manager to check the availability of the simulation model ("transceiver_as8221") and its hierarchical subcomponents (alphabetical order):
 - bus_guardian_interface
 - communication_controller_interface
 - cth
 - digital_logic
 - host_controller_interface

-
- ot_protection
 - power_supply_interface
 - receiver
 - rth
 - transceiver_as8221
 - transmitter
 - wakeup_detector
 - Include the library "as8221" in your test bench
 - LIBRARY as8221;
 - USE as8221.ALL;
 - Instantiate the model like highlighted in the attached example (see chapter 4) without the alias for "ELECTRICAL_REF".

3.2 ADVance MS 2006.2a

Installation guidance for ADVance MS is available on request.

3.3 SystemVision Professional 5.0 Build 2007.81

3.3.1 Library preparation

- Create a temporary folder and copy the file "AS8221_MGSV_5.0_V1.0.zip" into this folder
- Unzip "AS8221_MGSV_5.0_V1.0.zip"
- Create a folder within your simulation environment for the AS8221 simulation model library
- Move subfolder "AS221" into this folder

3.3.2 Library integration

- Open the Project Navigation Tree in SystemVision
- Activate the tab "Simulation" and change to "Model Libraries"
- Right mouse click at "HDL-Libraries"
- Add HDL library, browse and activate subfolder "AS8221"
- Library "AS8221" is now added within the HDL-Library tree and will contain the following models (alphabetical order):
 - BUS_GUARDIAN_INTERFACE
 - COMMUNICATION_CONTROLLER_INTERFACE
 - CTH
 - DIGITAL_LOGIC
 - HOST_CONTROLLER_INTERFACE
 - OT_PROTECTION
 - POWER_SUPPLY_INTERFACE
 - RECEIVER
 - RTH
 - TRANSCEIVER_AS8221
 - TRANSMITTER
 - WAKEUP_DETECTOR
- Include the library "as8221" in your test bench
 - LIBRARY AS8221;
 - USE AS8221.ALL;

Instantiate the model like highlighted in the attached example (see chapter 4).

3.4 Saber HDL 2007.12

3.4.1 Version details

- SaberHDL 2007.12.2.0SP2-4.0 Build 13 on 20-May-2008 Copyright 1985-2006 Synopsys, Inc.
- MAST 2007.12.2.0SP2-4.0 Build 13 on 20-May-2008 Copyright 1985-2006 Synopsys, Inc.

3.4.2 Install guide Saber (Linux Systems)

- Select working directory
- Unzip Zip file
- Configuration files and source folders:
 - Folder "model_source": Encrypted source files for transceiver model
 - Folder "thermal_source": Encrypted source files for thermal network
 - Folder "testbench": Encrypted source files for test bench generation
- Compile scripts:
 - "compile_as8221.ai_vhdsn": Generation of AS8221 lib element
 - "compile_thermal_lib.ai_vhdsn": Generation of thermal elements
 - "compile_testbench.ai_vhdsn": Generation of test bench elements
- Symbols:
 - transceiver_AS8221.ai_sym (transceiver symbol)
 - capacitor.ai_sym (capacitor symbol)
 - resistor.ai_sym (resistor symbol)
 - simple_wire.ai_sym (simple net symbol)
 - pwl.ai_sym (pwl source symbol)
 - gnd.ai_sym (ground symbol)

3.4.3 Generation library "work"

- Call "saberhdl" from working directory
 - File -> Open -> Design
- "Open Design" Dialog -> Load
 - Select "compile_as8221.ai_vhdsn"
 - Select "Compile" button
 - Modify file sources directory to working directory/model_source
 - Select "transceiver" for "Root Entry"
 - Select working directory for "Directory" -> Very important to select the correct one!
 - Select "work" for "Compile Persistent Library"¹
 - Press OK
 - (If error occur e.g. "cannot open library work" just repeat the step before once)
- Library elements for model as8221 will be created

3.4.4 Generation of thermal elements library

- Same steps like before in chapter 3.4.3
 - Use "compile_thermal_lib.ai_vhdsn"
- Library for thermal elements will be created

3.4.5 Generation of test bench elements library

- Same steps like before in chapter 3.4.3
 - Use "compile_testbench.ai_vhdsn"

¹ ATTENTION: Saber sketch has currently NO possibility to select another library than "work"

- Library for test bench elements will be created

3.4.6 Utilization of symbols

- Call "sketch" from working directory
 - File -> New -> Schematic
- Schematic -> Get Part -> By Symbol Name
- Get and Place Symbol By Name -> Browse
- Select symbol
 - Select "transceiver_AS8221.ai_sym"
 - Open
- Place (in Get and Place dialog)
- Set parameters
- Select architecture

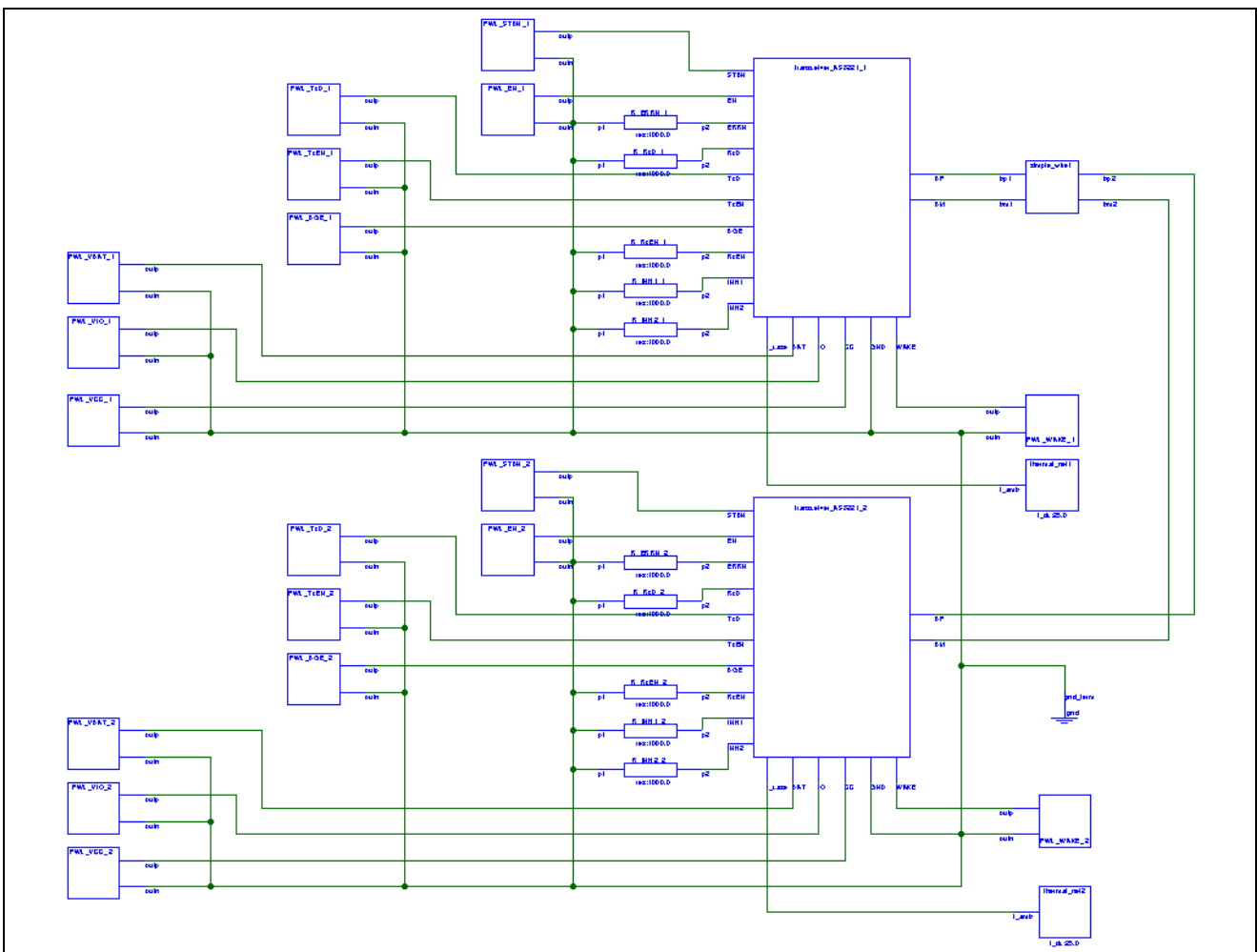


Figure 1: Test bench example in Saber Sketch

3.4.7 Apply simulation with schematic in Saber Sketch

- Edit -> SaberHDL/Netlisting Settings -> Add Search Path
 - Alias - Path
 - AS8221 - ./model_source
 - Thermal - ./thermal_source
 - Bench - ./testbench

- Design -> use your schematic
- Simulator -> SaberHDL
- Netlist your schematic
- Simulate your schematic

3.4.8 Analyses

- Time-Domain -> Operating Point/Transient
 - Use std. settings
 - Simulation time: 400.0 ms
 - Step size: 10.0e-9
- Watch simulation reports
 - Set debug_flag in transceiver model = true
 - Set instance_nr to number of transceiver instance
 - Open Saber Guide
 - Watch simulation console

4 Instantiation Examples

4.1 Example for network definitions

```
terminal    t_amb, t_i_1, t_i_2, t_case_1, t_case_2 : thermal;

terminal    BP, BM : electrical;
terminal    BAT_1, CC_1, IO_1, WAKE_1, STBN_1, EN_1, ERRN_1, RxD_1,
            TxD_1, TxEN_1, BGE_1, RxEN_1, INH1_1, INH2_1 : electrical;

terminal    BAT_2, CC_2, IO_2, WAKE_2, STBN_2, EN_2, ERRN_2, RxD_2,
            TxD_2, TxEN_2, BGE_2, RxEN_2, INH1_2, INH2_2 : electrical;

quantity    v_bus across BP to BM;

alias       ground is ELECTRICAL_REF;
```

4.2 Example for model instantiation

```
transceiver_1: entity transceiver_as8221(behav)
generic map(
  r_open          => 1.0e6,      -- off resistance of switch [Ohm]
  r_closed        => 1.0e-3,     -- on resistance of switch [Ohm]
  rise_time       => 10.0e-9,   -- switching time [s]
  fall_time       => 10.0e-9,   -- switching time [s]
  v_BGE_H_ratio   => 0.7,       -- BGE high level input voltage (ratio of Vio)
  v_BGE_L_ratio   => 0.3,       -- BGE low level input voltage (ratio of Vio)
  v_RxEN_H        => 4.0,       -- RxEN high level output voltage
  v_RxEN_L        => 0.4,       -- RxEN low level output voltage
  v_TxD_H_ratio   => 0.7,       -- TxD high level input voltage (ratio of Vio)
  v_TxD_L_ratio   => 0.3,       -- TxD low level input voltage (ratio of Vio)
  v_TxEN_H_ratio  => 0.7,       -- TxEN high level input voltage (ratio of Vio)
  v_TxEN_L_ratio  => 0.3,       -- TxEN low level input voltage (ratio of Vio)
  v_RxD_H         => 4.0,       -- RxD high level output voltage
```

<i>v_RxD_L</i>	=> 0.4,	-- <i>RxD low level output voltage</i>
<i>t_sleep</i>	=> 40.0e-6,	-- <i>timeout to switch to sleep mode</i>
<i>t_TxEN_timeout</i>	=> 2.0e-3,	-- <i>timeout for asserted TxEN</i>
<i>v_STBN_H_ratio</i>	=> 0.7,	-- <i>STBN high level input voltage (ratio of Vio)</i>
<i>v_STBN_L_ratio</i>	=> 0.3,	-- <i>STBN low level input voltage (ratio of Vio)</i>
<i>v_EN_H_ratio</i>	=> 0.7,	-- <i>EN high level input voltage (ratio of Vio)</i>
<i>v_EN_L_ratio</i>	=> 0.3,	-- <i>EN low level input voltage (ratio of Vio)</i>
<i>v_ERRN_H</i>	=> 4.0,	-- <i>ERRN high level output voltage</i>
<i>v_ERRN_L</i>	=> 0.4,	-- <i>ERRN low level output voltage</i>
<i>t_ro_en_timeout</i>	=> 50.0e-6,	-- <i>read-out enable timeout [sec]</i>
<i>t_ro_prop_errn</i>	=> 100.0e-9,	-- <i>propagation delay EN -> ERRN</i>
<i>OT_th_H</i>	=> 165.0,	-- <i>over-temperature high threshold</i>
<i>OT_th_L</i>	=> 150.0,	-- <i>over-temperature low threshold</i>
<i>v_BAT_th_H</i>	=> 4.5,	-- <i>V_BAT undervoltage recovery threshold</i>
<i>v_BAT_th_L</i>	=> 3.5,	-- <i>V_BAT undervoltage detection threshold</i>
<i>v_CC_th_H</i>	=> 4.0,	-- <i>V_CC undervoltage recovery threshold</i>
<i>v_CC_th_L</i>	=> 3.0,	-- <i>V_CC undervoltage detection threshold</i>
<i>v_IO_th_H</i>	=> 1.6,	-- <i>V_IO undervoltage recovery threshold</i>
<i>v_IO_th_L</i>	=> 1.1,	-- <i>V_IO undervoltage detection threshold</i>
<i>t_uv_detect</i>	=> 0.1,	-- <i>undervoltage detection time</i>
<i>t_uv_recover</i>	=> 0.1,	-- <i>undervoltage recovery detection time</i>
<i>v_bus_active_h</i>	=> 225.0e-3,	-- <i>activity detection high threshold</i>
<i>v_bus_active_l</i>	=> -225.0e-3,	-- <i>activity detection low threshold</i>
<i>t_bus_activity_detect</i>	=> 200.0e-9,	-- <i>activity detection time</i>
<i>t_bus_idle_detect</i>	=> 100.0e-9,	-- <i>idle detection time</i>
<i>v_data0</i>	=> -225.0e-3,	-- <i>data 0 detection threshold</i>
<i>v_data1</i>	=> 225.0e-3,	-- <i>data 1 detection threshold</i>
<i>t_bus_RxD_01</i>	=> 40.0e-9,	-- <i>delay from bus to RxD (0->1)</i>
<i>t_bus_RxD_10</i>	=> 40.0e-9,	-- <i>delay from bus to RxD (1->0)</i>
<i>i_limit</i>	=> 100.0e-3,	-- <i>bus current limit</i>
<i>t_BUS_ERROR</i>	=> 20.0e-9,	-- <i>bus error detection time</i>
<i>i_BP_th_L</i>	=> 5.0e-3,	-- <i>BP current lower threshold</i>
<i>i_BP_th_H</i>	=> 40.0e-3,	-- <i>BP current higher threshold</i>
<i>i_BM_th_L</i>	=> 5.0e-3,	-- <i>BM current lower threshold</i>
<i>i_BM_th_H</i>	=> 40.0e-3,	-- <i>BM current higher threshold</i>
<i>v_diff_active</i>	=> 225.0e-3,	-- <i>bus differential min active voltage</i>
<i>Vbat_wake_min</i>	=> 4.0,	-- <i>min battery voltage for enabling wake-up</i>
<i>t_BWU_0</i>	=> 4.0e-6,	-- <i>(bus wake-up) 0 min hold time</i>
<i>t_BWU_1</i>	=> 4.0e-6,	-- <i>(bus wake-up) 1 min hold time</i>
<i>t_BWU_timeout</i>	=> 48.0e-6,	-- <i>(bus wake-up) wake sequence timeout</i>
<i>v_WU_1</i>	=> 300.0e-3,	-- <i>(bus wake-up) 1 min bus voltage</i>
<i>v_WU_0</i>	=> -300.0e-3,	-- <i>(bus wake-up) 0 max bus voltage</i>
<i>v_LWU_thr</i>	=> 3.0,	-- <i>(local wake-up) WAKE threshold voltage</i>
<i>t_LWU_filter</i>	=> 10.0e-6,	-- <i>(local wake-up) filtering/hold time</i>
<i>instance_nr</i>	=> 1,	

```
    debug_flag          => false)

port map(
  GND          => ground,
  BAT          => BAT_1,
  CC           => CC_1,
  IO           => IO_1,
  WAKE         => WAKE_1,
  BP           => BP,
  BM           => BM,
  STBN         => STBN_1,
  EN           => EN_1,
  ERRN         => ERRN_1,
  RxD          => RxD_1,
  TxD          => TxD_1,
  TxEN         => TxEN_1,
  BGE          => BGE_1,
  RxEN         => RxEN_1,
  INH1         => INH1_1,
  INH2         => INH2_1,
  t_case       => t_case_1);
```